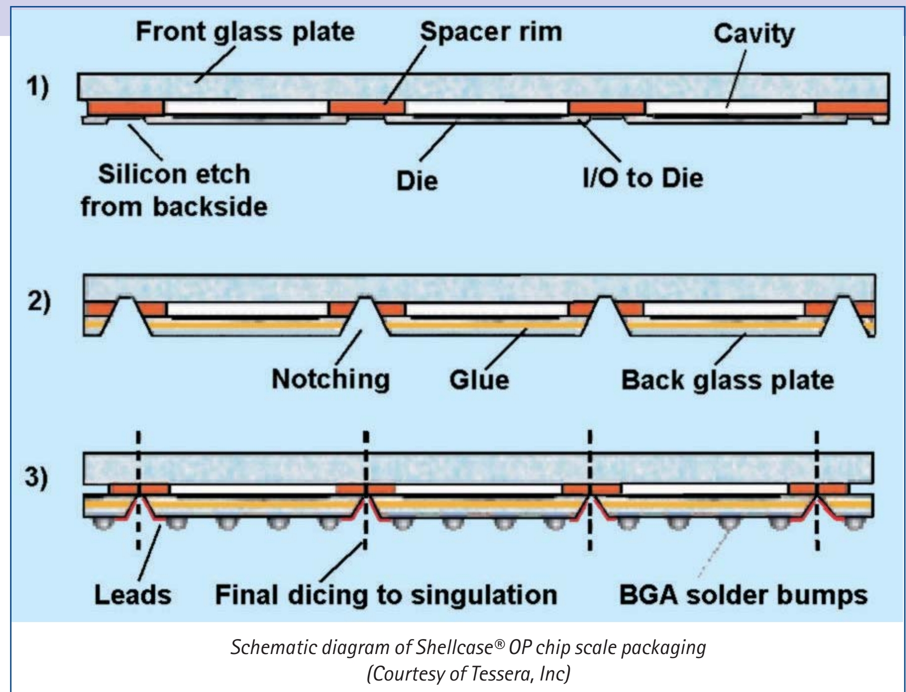
Plasma Etching in Packaging Applications

The assembly and packaging equipment and materials market is a significant part of the global semiconductor market totaling around US$13.6 million in 2004. The rapid adoption of technologies such as wireless, MEMS and optoelectronics into high volume consumer products has proved a strong driver for advances in packaging innovations such as System in a Package (SIP), System on Chip (SOC), Wafer Level Packaging (WLP) and System on Package (SOP). The latest techniques aim to integrate different functions, such as MEMS sensors, RF components , optoelectronics and memory storage on one chip.



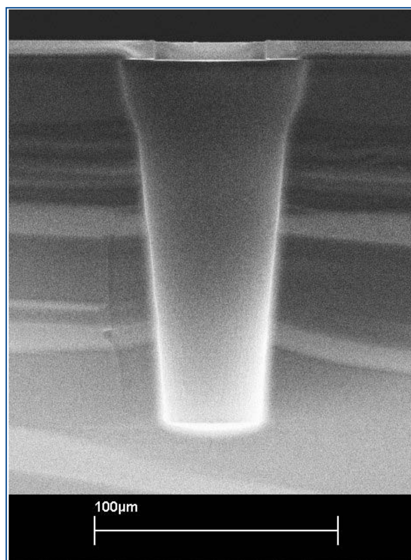
Schematic diagram of Shellcase® OP chip scale packaging (Courtesy of Tessera, Inc)

Etching of silicon structures with sloped sidewalls

STS has worked with a number of customers whose wafer-level packaging processes require etching of sloped or tapered silicon structures. A sloped step allows the metal film to be deposited and patterned without risk of discontinuities or excessive thinning. This technique is currently being used in the volume production of image sensors such as camera chips for mobile phone hand-sets[1]. In these applications the etching process recipe is adjusted to balance the competing etching and deposition components in the plasma. The process gas comprises a mixture of an etching gas (for example, SF_6) and polymer deposition gas (C_xF_y). In the plasma, a continuous balance between silicon etching by F atoms and fluorocarbon polymer deposition at the sidewalls is maintained such that a lateral etching rate having some fixed fraction of the vertical etching rate is obtained. By adjusting the ratio between the vertical and lateral etching rates, a specific sidewall slope angle can be achieved. In practice, the process requires adjustment for specific wafer types, since the vertical and lateral silicon etching rates depend to differing degrees on the total exposed silicon area and the mask material. To reduce the sidewall slope (i.e. etch shallower sidewall angles):

- Reduce polymer deposition gas flow
- Reduce wafer bias voltage
- Increase wafer susceptor temperature
- Increase etching gas flow

SEM image of backside sloped sidewall silicon etch in Shellcase® OP chip scale packaging (Courtesy of Tessera, Inc.)



Tapered silicon via hole etched using two-step SF_6/O_2 plasma process to eliminate overhang at the top of the via. Etch rate = 14µm/min

These adjustments permit some tuning of the sidewall angle, allowing process optimization for individual pattern configurations. However, in practice, these complex interactions require a compromise between the ideal profile angle and an acceptable average etching rate[2]. In STS' Pegasus tool, etch rates have been increased to over 15µm/min compared to ~8µm previously acheived in the "ASE-HR" system.

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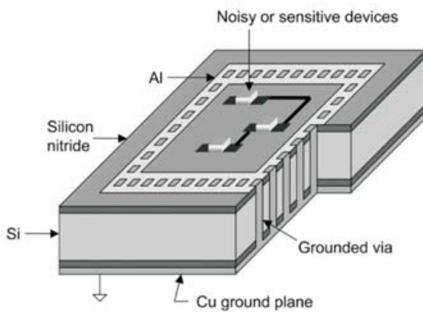
Deep Reactive Ion Etching (DRIE) for through wafer interconnects

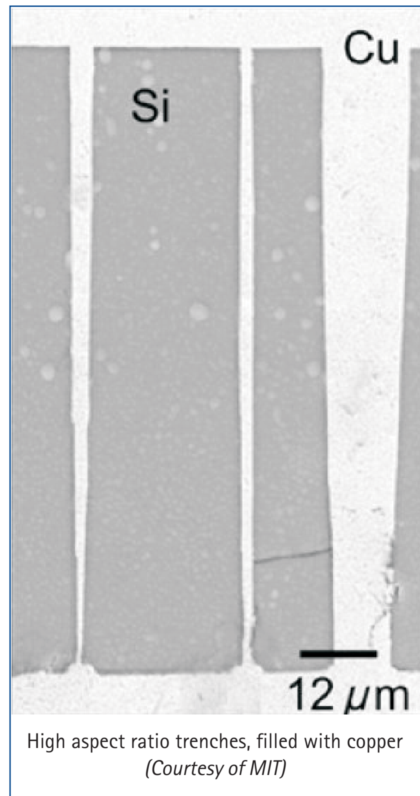
Deep Reactive Ion Etching is a time-multiplexed etching process patented in the mid-1990s by Robert Bosch GmbH. It comprises of sequential plasma etching and deposition steps, which generate an approximately vertical silicon sidewall. This basic concept originally aimed at the MEMS market has evolved continuously over the years and now extremely high performance silicon micro-machining processes are offered by STS.

The same process is now attracting growing interest for the packaging of MEMS devices, systems-in-package (SiP) and 3D-integrated circuits which are currently the focus of wide-ranging and intensive development activities.

One such example was illustrated by work carried out by researchers at Massachusetts Institute of Technology (MIT), who fabricated a "Faraday cage" structure to suppress substrate cross-talk in system-on-chip applications [3]. They used STS DRIE processing to etch a ring of high aspect ratio vias (lined with SiN and filled with copper) around a noisy or sensitive device in the chip



Schematic diagram of the Faraday cage arrangement used to suppress cross-talk.

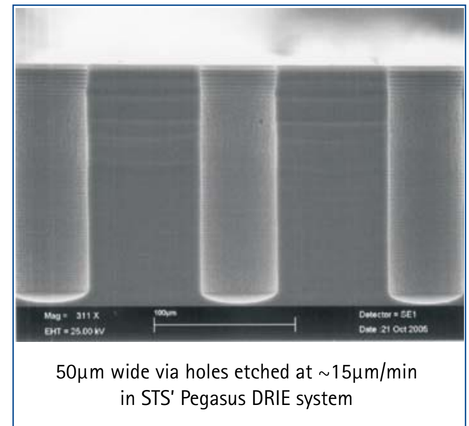


High aspect ratio trenches, filled with copper *(Courtesy of MIT)*

In Taiwan, researchers from National Tsing Hua University have used STS DRIE processing to fabricate vias through 550μm thick silicon wafer, using a aluminum hard mask, and infilled with thermal oxide and electroplated copper. MEMS micro temperature sensors were fabricated on the frontside of the wafer and solder bumps were then directly electroformed (using photoresist moulds) onto the copper interconnections[4] (see above).

Optimizing sidewall smoothness in via etching using DRIE

Since the silicon micro-machining process comprises of sequential etching and deposition steps, the etched sidewalls exhibit characteristic horizontal artifacts (frequently termed "scallops") corresponding to the beginning and end of each etching step. These "scallops" are a well-known characteristic of the Bosch-type process. While vias etched through silicon for SiP applications do not require a surface finish as smooth as that demanded for optical switching applications, the condition of the via sidewall can impact the performance of the subsequent metal seed-layer deposition process. Length of etch and passivation steps, and the intermixing of the etching and deposition gases in the transition from one step to the other, has been found to increase the average scallop size. Therefore both the HRM and Pegasus DRIE sources from STS have been engineered to allow very short switching times, which limits amount of lateral etching occurring in each etch step while maximizing the overall etch time and thus the overall etch rate.



50μm wide via holes etched at ~15μm/min in STS' Pegasus DRIE system

References

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[2] S. Heraud, C. Short and H. Ashraf, Proceeding of 59th Electronic Components and Technology Conference (ECTC2009), San Diego

[3]J.H. Wu, J. Scholvin and J. A del Alamo, IEEE Transactions on Electron Devices, Vol 51 number 11 Nov 2004

[4] C.-J. Lin, M.-T. Lin, S.-P. Wu and F.-G. Tseng, Journal of Microsystem Technologies, Volume 10, No 6-7, Oct 2004

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