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DREM2: a facile fabrication strategy for freestanding three dimensional silicon micro- and nanostructures by a modified Bosch etch process

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Abstract

Three dimensional (3D) silicon micro- and nanostructures enable novel functionalities and better device performances in various fields. Fabrication of real 3D structures in a larger scale and wider applications has been proven to be limited by the technical difficulties during the fabrication process, which normally requires multiple process steps and techniques. Direct top-down fabrication processes by modifying a plasma etch process have been proposed and studied in previous studies. However, the repeatability, size uniformity and the maximal number of stacked layers were limited. Here we report a facile single run fabrication strategy for three dimensional silicon micro- and nanostructures. A good uniformity of suspended layer thickness has to be achieved and up to 10 stacked layers have been fabricated in a single run without other additional steps or post-process procedures. This is enabled by a modified multiplexed Bosch etch process, so called DREM (deposit, remove, etch, multistep), while the DREM etch is used to transfer the patterns into silicon, an extra isotropic etch creates a complete undercut and thus freestanding structures come into form. This method is easy to program and provides well-controlled etch profiles.

Keywords: DRIE, DREM, silicon, plasma etching, Bosch process, three dimensional structures

(Some figures may appear in colour only in the online journal)

1. Introduction

Three dimensional (3D) silicon micro- and nanomachining has attracted a lot of interest in recent years for both research and industrial uses, and several promising applications have been proposed and demonstrated, e.g. vertically stacked silicon nanowires for field effect transistors (FET) [1], unified memory [2] and biosensors [3], shape-modified silicon nanopillars for quantum transport study [4] and FET [5], 3D silicon single cubic structures for 3D photonic crystal structures [6], etc. However, to easily fabricate 3D micro- and nanostructures, and simultaneously obtain a good size and shape control of the fabricated structures, is still considered to be difficult.

Bottom-up methods can create single crystalline silicon nanostructures, and the morphology can be encoded [6], however, this method is difficult to be integrated in traditional complementary metal-oxide-semiconductor (CMOS) industries. Top-down approaches, which can transfer the 2D lithography patterns into silicon in a 3D structure have been studied extensively before, e.g. using wet etching [7, 8], or more commonly, plasma etching (also called dry etching). Some of the dry etching methods reported before rely on an additional oxidation procedure to protect the sidewall of the structures during the dry release step [9, 10], however, the oxidation step and bottom opening step add extra fabrication complexity. Some other studies make use of the scallops

generated during a Bosch process and the self-limited oxidation process [3], however, the removal of the oxide layer after the etching process requires special techniques, such as vapor release or critical drying release, especially for nanostructures, which are easily collapse under capillary forces.

Here we report an improved fabrication method for 3D silicon micro- and nanostructures based on a previous paper by the authors [11], which require only one single plasma run without additional oxidation procedure or post-process steps. The 2D patterns are first defined with traditional ultraviolet (UV) lithography or electron beam lithography. Afterwards, the patterns are transferred into silicon with a modified plasma process, which consists of a DREM (deposit, remove, etch, multistep) process to sculpture structures and an extra isotropic etch step to release the structures. Instead of oxide, a fluorocarbon (FC) layer is used to protect the sidewall during the dry release step. The FC layer is generated directly during the same run by octafluorocyclobutane (C_4F_8) gases, which is a widely used as a passivation gas for Bosch etch processes. Thus, by tuning the etch process parameters during a single run, 3D structures can be created conveniently. This strategy has been tested for both micro- and nanostructures with different pattern designs, e.g. ultralong microcantilever (width of 1.5 μm, thickness of 500 nm and length of 400 μm) and multilayer silicon nanobeams (width of 20 nm, thickness of 50 nm and length of 2 μm) could be fabricated with this method. Besides, up to 10 stacked layers could be achieved showing good size uniformity and mechanical stability. Our approach allows for relatively low fabrication cost and high structure quality, which will open possibilities for novel device designs and applications.

2. Method

The patterns were defined by UV lithography for microstructures and electron beam lithography for nanostructures, and then transferred into silicon by deep reactive ion etching (DRIE). The technical details of the process flow are described as below.

The UV lithography was carried out with maskless lithography (MLA100, Heidelberg Instruments), which is a direct writing system with a high power LED light source (10 W at 365 nm). Different patterns were designed, and the negative photoresist AZ nLOF 2020 (MicroChemicals) was used, resulting in a resolution of resolution of around 1 μm. The thickness of the resist was 1.5 μm, and the dose during the exposure was 220 mJ cm^{-2}.

The electron beam lithography was performed with an electron beam writer (Jeol JBX-9500FS, JEOL) and the resist used was hydrogen silsesquioxane (HSQ, XR 1541 002 from Dow Corning). The thickness of the resist was around 100 nm, the acceleration voltage during exposure was 100 kV and the beam current was set to be 10 nA, which allows a small spot size (below 5 nm) and thus high resolution. The dose was around 20 000 μC cm^{-2}. The HSQ pattern is in many ways similar to silicon oxide and therefor can serve as a hard mask for the subsequent etch process. To verify the critical dimension of the exposed patterns, the samples were characterized by scanning electron microscopy (SEM, Supra V60, Zeiss).

The etching process was performed in an inductively coupled plasma (ICP) etching system (DRIE Pegasus, SPTS), and the processing details will be discussed in details in next section. The sample chips were attached on a carrier wafer, which is a 150 mm single side polished silicon wafer coated with 100 nm thick alumina by atomic layer deposition (R200 ALD system, Picosun). After etching, the samples were cleaned with oxygen plasma in a plasma asher system (TePla 300, PVA TePla).

3. Results and discussions

3.1. 3D silicon microstructures

The basic principle to fabricate 3D silicon micro- and nanostructures is based on the DREM process as introduced in [12]. Briefly speaking, a DREM process is a three-step Bosch process, which enables a better control of etch process [13]. Compared with typical two-step Bosch process with deposition step and etch step, the DREM process introduces a bottom removal step as shown in figure 1(a). During deposition step, C_4F_8 gas is applied without bias to create an almost conformal coating on both sidewalls and the bottom. Subsequently, in the 'removing' step, argon is used with high bias to clean the FC layer in the bottom. Since this step is performed in at low pressure, a high anisotropicity can be achieved and the FC layer on the sidewall remains unaffected. Then SF_6 gas is used to etch the silicon, this step is performed without bias, resulting in a small scallop size limiting sidewall roughness. This special three-step DREM process provides excellent sidewall protection, and, while keeping the scallop size small, a highly anisotropic etch profile can be achieved for freestanding structures.

Having the DREM process, to sculpture anisotropic etch profiles with high sidewall protection, we can now create 3D structures by adding an extra isotropic etch in the total sequence as introduced before in [14–16]. The process flow is shown in figure 1(b). First the patterns were defined by traditional UV lithography, afterwards an anisotropic etch profile was created by a number of DREM cycles, then an isotropic etch was applied to provide an undercut to the anisotropic structures. These structures will then be freestanding and act as a mask for the second round of DREM process steps and another isotropic etch. Since the sidewalls of the anisotropic structures are well protected, the iteration of DREM processes followed by an isotropic etch could be repeated several times, thus more freestanding layers (each layer is defined by one DREM cycle) could be fabricated without collapse of the structure. A technical challenge during the process is the precise control of the geometry of the structures, e.g. to fabricate all the the layers with an identical thickness (i.e. exact same etch depth per cycle independent of the aspect ratio). This is crucial for the fabrication of 3D structures that suitable for practical applications. In our study, this technical issue is solved by applying a process parameter ramping technique.
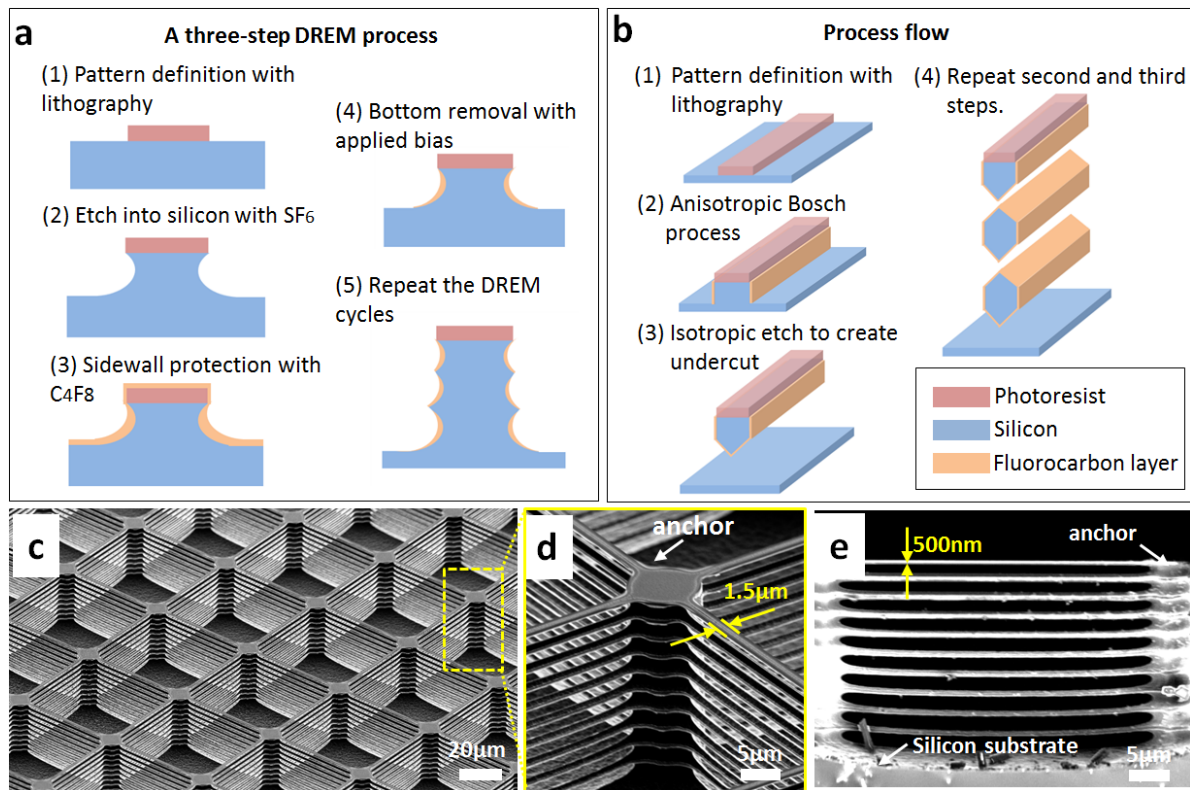
Figure 1. (a) A schematic view of a three step DREM process; (b) process flow for fabrication of 3D silicon structures; (c) SEM image of a 3D silicon microstructures with 10 isolated stacked layers, (d) zoom in of the region in (c), which shows the anchor part that holds 10 stacked silicon beams, (e) a cross section view of the 3D silicon structures.

The process parameter ramping technique has been introduced in a previous paper [12], in which a sausage-chain-like micropillar structures were fabricated. It is well known that the etch rate of silicon is aspect ratio dependent, the effect is known under ARDE (aspect ratio dependent etch rate) or sometimes just referred to RIE lag [17, 18]. In our case, both the etch rate during each cycle of the DREM process and the isotropic etch rate will slowly decrease as the etch process progresses down into the silicon. This causes a decreasing size of the scallops, which we documented in a previous study [12]. This issue becomes particularly significant when we want to create a number of suspended (freestanding) layers. To compensate for this effect, we slowly increase the time of the etch cycle in our DREM process, so the scallop size will be constant down into the silicon, and an excellent thickness uniformity of the different suspended layers can be achieved. At the same time, the duration of the isotropic etch cycle is also increasesed, thus the size of the gap between each two suspended layers is identical. This parameter ramping procedure is crucial in order to have precise size control of the fabricated 3D structures, which is otherwise difficult and cumbersome with alternative fabrication techniques. All the parameter settings are shown in table 1.

Figure 1(c) is a SEM image of a 3D silicon microstructure fabricated with the presented DREM, and isotropic etch process, consisting of 10 suspended layers of beam structures supported by pillars, which are larger in size and act as anchors, so the isotropic etch step will not undercut and release the whole structure. An enlarged view is shown in figure 1(d), where we can clearly see the suspended beams (with a width

of 1.5 μm, and length of 50 μm), and the vertical supporting anchors (with a diameter of 10 μm). A cross section view is shown in figure 1(e), where we can see the suspended beams, which have a uniform thickness of around 500 nm, and the gaps between each two suspended layers also have a uniform size of around 2.5 μm.

By applying the fabrication technologies discussed above, different kinds of freestanding structures can be fabricated. In figure 2 there are three kinds of structures etched from the same mask design, which is a double spiral structure with anchors and beams (with a linewidth of 2 μm). Three different fabrication sequences were applied as shown in figure 2(d). Figure 2(a) shows a cantilever like beam structure, which is fabricated by 10 cycles of the DREM process followed by an isotropic etch release. Figure 2(b) shows capacitor-like structures, which are etched by 50 cycles followed by a final isotropic etch step. Figure 2(c) shows five isolated structures, each layer is etched with 10 cycles of the DREM process followed by an isotropic etch, giving a thickness of around 2 μm for each isolated layer. From the results we can see the flexibility of this approach, which makes fabrication easy to program for different applications. However, it should be noted that, in order to have a uniform size distribution of different suspended layers, the etch speed should be controlled precisely, so the scallop size distribution is uniform (as shown in figure 3(e)). This is accomplished by the parameter ramping technique discussed earlier.

By designing the patterns properly, different structures with complicated pattern designs can be fabricated as presented in

Table 1. An overview of parameter settings to create 3D silicon microstructures.

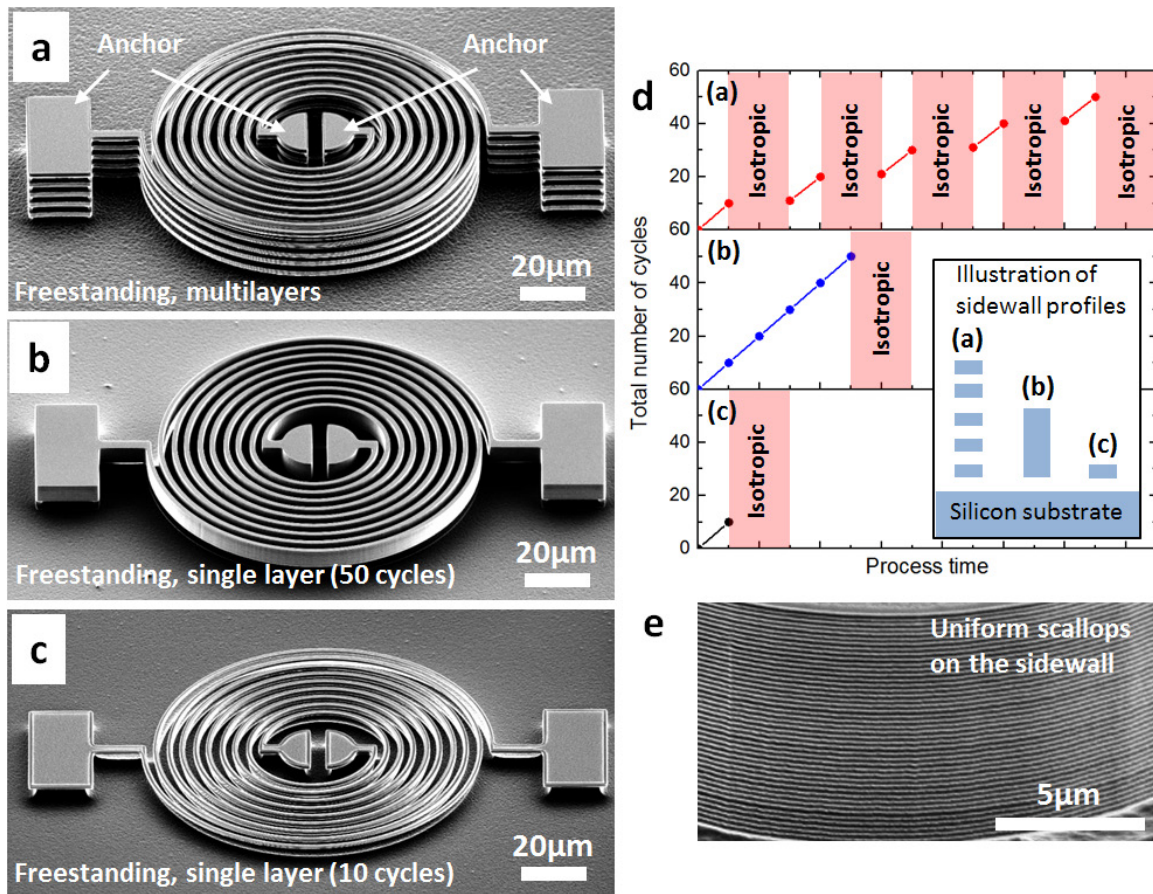|	DREM process step			Isotropic etch step
	Deposition	Bottom removal	Etch	
Time (s)	1.0	0.5	Ramping up from 2.5 s ramping rate: 0.5 s/cycle	Ramping up from 10 s ramping rate: 0.5 s/cycle
C_4F_8 gas flow (sccm)	400	5	5	5
SF_6 gas flow (sccm)	15	15	600	600
Argon gas flow (sccm)	250	75	250	250
Coil power (W)	3000	3000	3000	3000
Platen power (W)	0	300	0	0
Pressure (mTorr)	20	5	20	20
Temperature (°C)	−19	−19	−19	−19

Figure 2. Different strategies to create freestanding structures: (a) one suspended layer which consists of 10 Bosch cycles; (b) one suspended layer which consists of 50 Bosch cycles; (c) five suspended layers, each layer consists of ten Bosch cycles; (d) a schematic view of the processes in (a)–(c), and an illustration of cross section view of the structures in the inset; (e) a zoom in view of the scallops on the sidewall of structures in (b).

figure 3. Five sequences of ten DREM cycles each followed by an isotropic etch were performed in (a)–(c). Figure 3(a) shows arrays of spiral-like structures with the anchor in the middle, the linewidth of the suspended beams is 2 μm, and the gap between the beams is 2 μm. Figure 3(b) shows arrays of stacked ring resonator-like structures with different diameters, the linewidth of the ring is 2 μm. Figure 3(c) shows arrays of tuning fork-like structures with different length from 20 μm to 200 μm, the linewidth of the suspended beams is 2 μm. An enlarged section of the image is shown for each structure,

which gives more details regarding the isolated layers. In figure 3(d) we show a 3D photonic crystal-like structure, which is created by six sequences of five DREM cycles each followed by an isotropic etch. The fabricated structure has six stacked layers of holes with a square lattice type, the diameter of the holes is 3 μm and the periodicity is 4 μm (an enlarged view of the structures are shown in figures 3(e) and (f)). A simple illustration is also shown in the bottom left corner of the image to show the anchors (blue) and suspended structures (yellow). This figure shows the flexibility of our fabrication
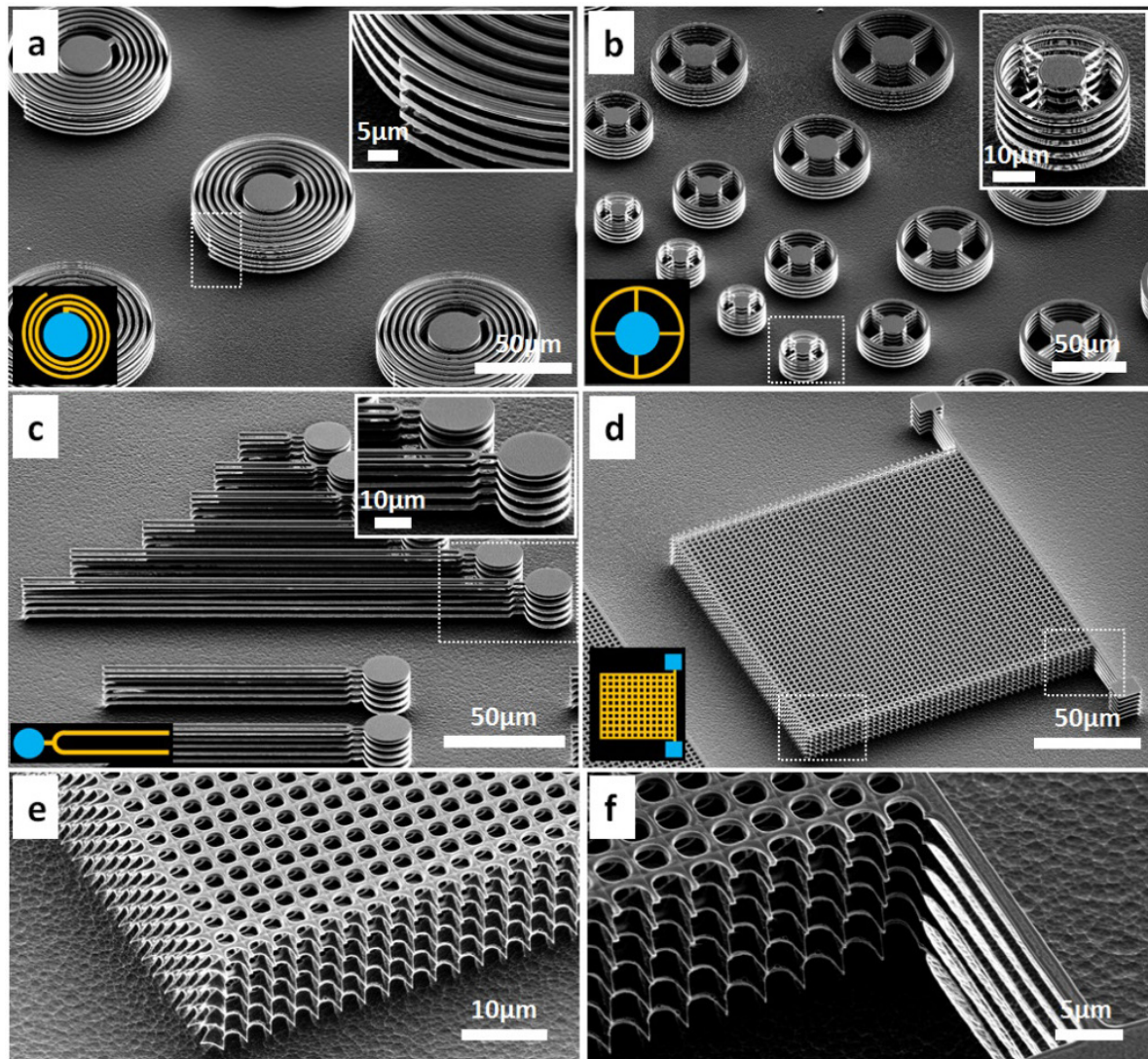
Figure 3. SEM images of different complex 3D microstructures (from (a) to (d)). A schematic view (bottom-left corner in each image) shows the anchor parts (blue) and the stacked layer parts (yellow). Zoomed in images are shown in the insets (top right corner) in (a)–(c), which show the details of the parts in dashed squares in the SEM images. Figures (e) and (f) are zoom in images from two regions labeled in (d).

technique, it also implies possibilities for various applications in photonics [19], micromechanics [20], etc.

It should be noted that the bottom part of anisotropic structures will be consumed slowly upwards during the isotropic etch step, which will change the thickness of the suspended structure and additional calculations are thus needed to have a precise size control of these structures. To illustrate the demolishing effect of isotropic etch on anisotropic structures, a wheel-like pattern with diameter of 500 μm is designed as shown in figure 4(c). The rim of the wheel and the 'spokes' have a linewidth of around 2 μm, and the whole structure is supported by an anchor in the center, which has a diameter of 15 μm. In the experiments, 20 DREM cycles were first applied to create anisotropic structures, and then an isotropic etch was applied with different durations of 10 s, 20 s and 30 s. It is found that the number of remaining scallops on the anisotropic structures decrease linearly with increased isotropic etch time (figures 4(a) and (b)), which suggested a constant

isotropic etch rate into the structures of 60 nm s^{-1} (in the anchor region) and 80 nm s^{-1} (in the rim region) as shown in figure 4(d). This phenomenon canbe explained qualitatively as follows: while the sidewall of the anisotropic structures is well protected by the FC layer, SF$_6$ based etching species will etch isotropically and undercut structures, thus the bottom of the structure is exposed to fluorine radicals and slowly gets thinner. This process is geometry (shape) dependent, resulting in the fact that the spokes and rims will be attacked from different directions after being released, thus the etch rate into structures will be higher than in the central support, where the isotropic etch can only attack the structure from one side. This phenomenon is important, since it will determine both the thickness of suspended structures and the size of the gap between two adjacent suspended layers, which are two important parameters to design 3D structure based devices. The anisotropic structures will be slowly etched away from the bottom, this will give a contribution to the final size of the
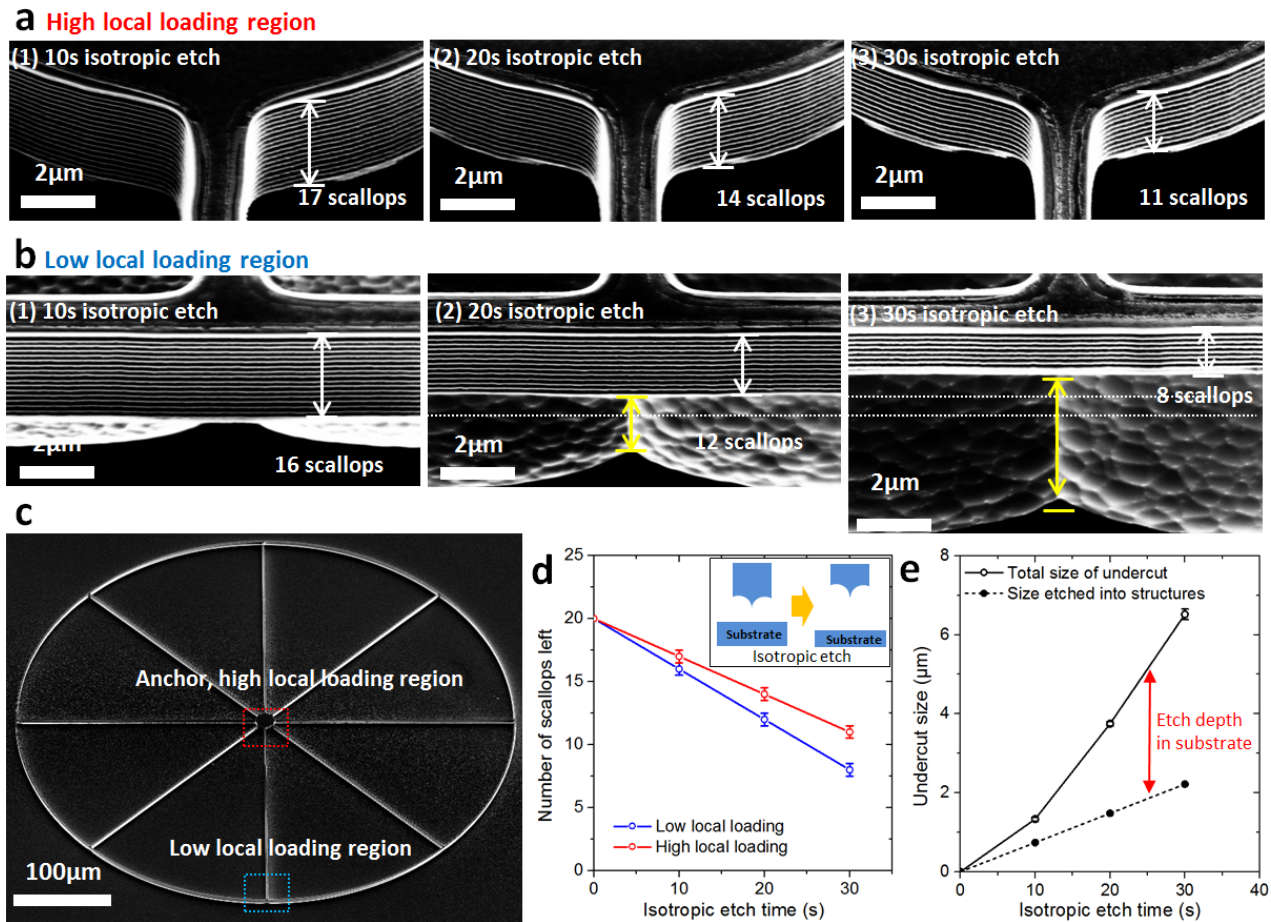
Figure 4. The influence of isotropic etch on freestanding structures. For regions with single-side isotropic undercut (a) and double-side isotropic undercut (b) with different isotropic etch time. The regions in (a) and (b) correspond to regions in the structure as shown in (c). The isotropic etch rates of the scallops being etched are shown in (d), with a schematic view of the structure change after isotropic etch process. The gap size between freestanding structures and the substrate is shown in (e).

gap (figure 4(e)) and thus should be considered during design. To give a practical example, in some cases a large gap size is favored, to achieve this, we should not just increase the isotropic etch time, since it will totally demolish the anisotropic structures. A more proper way, however, is to increase the number of cycles during the Bosch process, and in the same time increase the isotropic etch time.

By precisely controlling the isotropic etch step, we can fabricate some ultralong cantilever-like structures, which normally require silicon on insulator (SOI) wafers. In the latter the buried oxide layer is removed after the plasma etch. To prevent the structures from collapse due to the capillary force [21], some special techniques are needed, e.g. critical point drying after hydrofluoric (HF) solution removal [22], XeF$_2$ etching [23], vapor phase HF etching [24], or a C$_x$F$_y$-based plasma chemistry removal [25]. In our experiments, the undercut is created directly during the plasma etching process, thus the stiction effect can be avoided. Figure 5(a) shows two sets of cantilever structures, which were fabricated by 20 cycles of DREM followed by 22 s of isotropic etch. The width of the cantilever is around 1.5 μm (figure 5(b)), and the thickness of the cantilevers is around 300 nm, the lengths of the cantilevers are from 50 μm up to 500 μm, and they are completely free-hanging above from the substrate (figure 5(c)). The tips

of fabricated cantilever beams are also observed to clamp on the substrate during the scanning with SEM (figures 5(d) and (e)), which can be explained as the electrostatic attraction force caused by the charge accumulation on beams and substrates. This implies potential applications for switches and electrostatic actuations [26, 27]. This type of long cantilevers with thin thickness have also been demonstrated to have small spring constants to detect small forces [28] or to measure the mechanical properties of thin films coated on silicon [29]. This strategy is also promising to be fabricate free standing electronic devices, e.g. transformers and inductors [30].

3.2. 3D silicon nanostructures

While 3D microstructures can already bring new possibilities and applications in micromechanics, microelectronics, microfluidics, etc, to shrink the size further and create 3D nanostructures can give us novel insights into fundamental phenomena. This becomes very relevant when the CD of the structures is comparable to or below the wavelength of light, the mean free path of electrons or the electron phase coherence lengths. Compared with the methods to fabricate 3D silicon microstructures as discussed above, some additional technical issues need to be addressed for nanoscale, and the
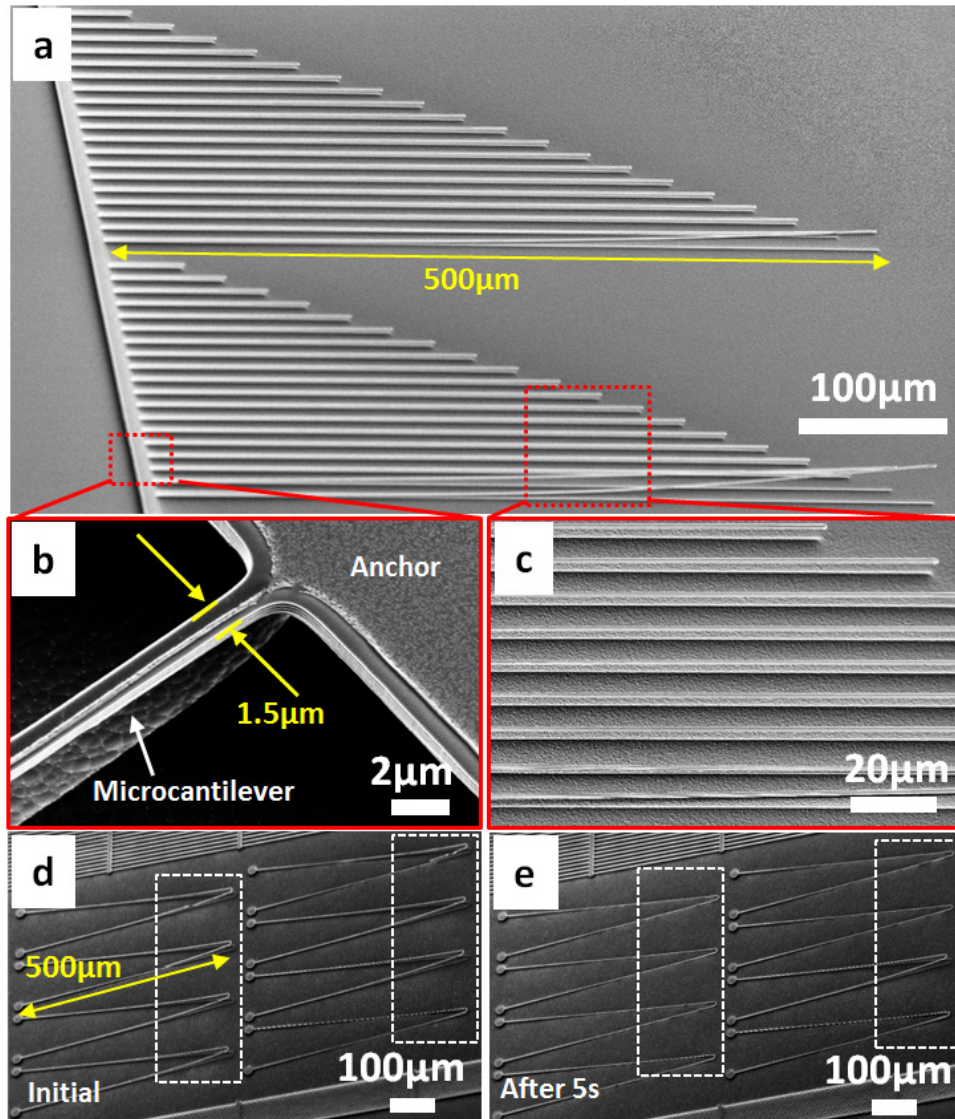
Figure 5. Ultralong silicon micocantilevers created with 20 DREM cycles followed by 22 s isotropic etch. (a) Cantilevers with length up to 500 μm; (b) an enlarged view of the anchor region of the cantilevers; (c) an enlarged view of the center of the cantilevers. Attaching phenomena for ultralong silicon microcantilevers under SEM, the initial morphology (d) and after 5 s (e).

major challenge is to have a profile control with higher precision, which is limited by the plasma etch process. Since the CD of the nanostructures can be below 100 nm,which is even smaller than the scallop size for already presented microstructures, the recipe has to be adapted to the these dimensions. Should the same recipe be applied as used for the microstructures, the large scallops and undercut will completely dissolve the nanostructures. In order to produce 3D nanostructures with this approach the etch rate needs to be significantly reduced, so that the sizes of scallops and undercuts can be minimized.

In table 2 we can see the parameter settings to create 3D nanostructures. In order to reduce the etch rate, the density of radicals should be decreased, thus a smaller coil power of 500 W is applied, and the gas flow ratio of SF_6 is also reduced [13]. By doing so a scallop size of around 15 nm could be achieved (compared with the large scallop size of around 200 nm for microstructures). The platen power is also reduced during the bottom removal step of DREM process, which

Table 2. An overview of parameter settings to create 3D silicon nanostructures.

	DREM process step			Isotropic etch step
	Deposition	Bottom removal	Etch	
Time (s)	0.4	1.0	2.5	1
C_4F_8 gas flow (sccm)	40	5	5	5
SF_6 gas flow (sccm)	10	10	30	30
Argon gas flow (sccm)	100	75	100	100
Coil power (W)	500	500	500	500
Platen power (W)	0	80	0	0
Pressure (mTorr)	6	3	6	6
Temperature (°C)	−19	−19	−19	−19

helps to reduce the roughness caused by resputtering, which is more crucial for nanostructures. The parameter ramping technique was not performed for the nanostructure etching, since
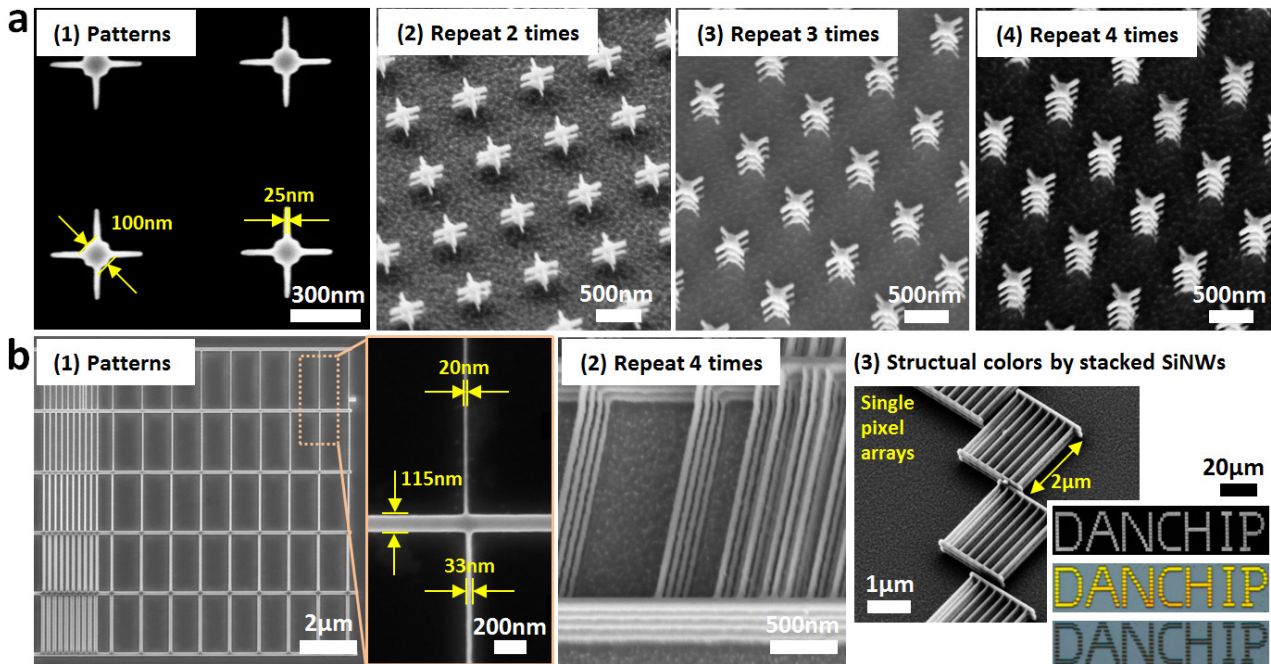
Figure 6. Fabrication of 3D silicon nanostructures: (a) cross-like structures defined by electron beam lithography (1), after plasma etching to create different number of stacked layers as shown in (2)–(4); (b) SEM images of SiNWs structures patterned by electron beam lithography (1), four stacked layers of SiNWs after etching (2), and single pixels made by two stack layers of SiNWs in (3), which can be used to make a graph that gives structural colors as shown in the bottom right corner, from top to bottom: SEM images, optical microscopic graph when the incident light polarization is perpendicular to the direction of SiNWs, and the optical microscopic graph when the incident light polarization is along the direction of SiNWs.

for nanostructures the aspect ratio is not as large as for the microstructures, thus the ARDE or RIE-lag is less prominent.

Some 3D silicon nanostructures are shown in figure 6. Electron beam lithography was used to define the high resolution patterns, which include cross-like structures (figure 6(a)(1)) and nanowire structures (figure 6(b)(1)), the smallest size of the patterns is around 20–25 nm, and larger patterns are defined to act as anchors for the suspended 3D structures. After several iterations of DREM and isotropic etch, 3D nanostructures are created from cross-like patterns (two stacked layers in figure 6(a)(2), three stacked layers in figure 6(a)(3), four stacked layers in figure 6(a)(4)), and nanowire patterns with four stacked layers in figure 6(b)(2). Five DREM cycles were applied during each anisotropic etch part, thus giving a height of around 50–60 nm for each layer of nanostructures, and the size of the gap between each two layers is around 50 nm. The line edge roughness (LER) of the HSQ patterns is measured to be below 3 nm, and the sidewall roughness is minimized by reducing the etch rate, thus the fabricated silicon nanowires (SiNWs) arrays in figure 6(b)(2) show a very good size uniformity, which is favorable for applications in nanophotonics and nanoelectronics, where the exact geometry of the structures is crucial. To briefly demonstrate one possible application of the 3D SiNWs, pixels were written (with pixel size of 2 μm by 2 μm) to form a graph, each pixel is composed of two stacked layers of SiNWs with linewidth of 50 nm, height of 50 nm, length of 2 μm and pitch of 300 nm as in figure 6(b)(3).These SiNWs have been shown previously to possess size and polarization dependent light scattering

properties, which can give enhanced light scattering intensity in certain wavelength regions [31, 32, 33]. In figure 6(b) (3), we can see such pixels could be used to write patterns with a high spatial resolution of around 10 000 dpi (dots per inch), which can give bright yellow structural colors when the polarization of light is perpendicular to the direction of SiNWs. When the polarization is rotated by 90°, the resonance mode is not active and thus no structural colors can be observed. Compared with previous studies on structural colors induced by light scattering of SiNWs [28, 29], our method does not rely on a complicated SOI structure, and the coupling of resonance mode from adjacent SiNWs could be extended to an extra dimension. Technical details of these light scattering properties of 3D SiNWs, however, is out of the scope of this paper and will be reported elsewhere.

4. Conclusion

3D silicon freestanding structures have been fabricated with a modified DREM (deposit, remove, etch, multistep) etch process without additional steps such as oxidation or wet releasing. Micro- and nanostructures were fabricated with excellent control of size uniformity and a maximum number of 10 stacked suspended layers. The process is reproducible and easy to program for different kinds of freestanding structures. Technical issues have been addressed and a three-step DREM process combined with parameter ramping, has been introduced. Some potential devices and applications have

been demonstrated, more practical applications based on this technique are under investigation.

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