# Micro 3W Experimental Semiconductor Technology

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## 1 Introduction

In micro- and nanofabrication, it is often desirable to create structures with straight side walls and an overall uniform appearance. This makes it possible to accurately reflect the pattern of the structures onto the substrate without any errors or transformations due to angles. In our project, we aim to optimize the process for making straight sidewalls to be used specifically for dry plasma etching. This is a problem Danchip researchers are actively working to solve as such geometry has been requested by companies using the facility.

Figure 1 shows an example of a nearly perfect structure as desired.

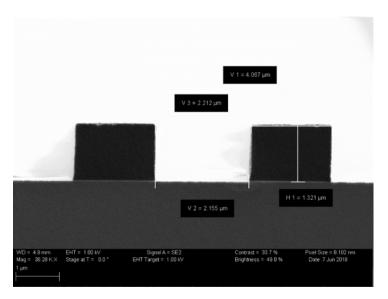


Figure 1: Example of ideal sidewall geometry

# 2 Theory

#### 2.1 Priming

To make it possible for the resist to stick to the substrate, a medium is needed to compensate for their different hydrophobic and hydrophilic abilities. The substrate is rather hydrophobic with a contact angle of around 70-80 degrees, while the resist is hydrophillic with a contact angle of around 10 degrees. A layer of is deposited onto the substrate which reacts with the substrate and binds to it while producing  $N_2$  as a bi-product. This requires some time to diffuse out of the substrate or you risk trapping it, thus creating bubbles.

#### 2.2 Spin-coating

After priming, the substrate is coated with a photosensitive resist. This resist is made from resin, solvent and a photo-active compound that gives the material it's photosensitive properties. A nozzle on the spin coater deposits a small quantity of resist onto the surface of the substrate, before the base spins at 4,600 rpm to evenly distribute the resist over the surface of the wafer.

#### 2.2.1 Edge Bead

During spin coating, a thicker region of resist forms near the outer edge of the substrate, this is known as an edge bead. Figure 2 shows the process of spin coating and the subsequent formation of an edge bead during the process.

In many cases, it is desirable to remove this edge bead as it can cause problems later in the process, for this an edge bead remover is used. This is a piece of equipment with a small nozzle that sprays a strong solvent onto the perimeter of the wafer, dissolving the edge bead.

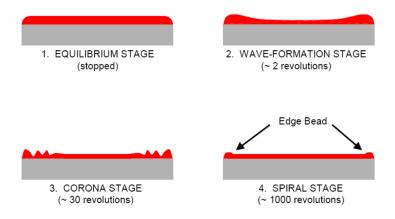


Figure 2: Formation of edge bead during spin coating process [2]

#### 2.3 Exposure

Here the photoactive part of the resist reacts to a given dose of exposure in the form of short wave-length light around typically 300-400 nm. The dose is the product of the exposure time and intensity. Depending on whether the resist is positive or negative, the exposure either makes the resist weaker or stronger, respectively.

Firstly a photomask is mounted between the wafer and exposure source, so that a pattern on the photomask is replicated in the resist part of the wafer. The pattern is decided by where light can and can't go through so it can be seen as windows in the mask. With the positive resist the pattern on the mask will be transferred directly from the mask to the resist but with negative resist the inverted form of the pattern is transferred. In our experiments the focus was on positive resist.

There are different parameters to work with when exposing the resist. The parameters are the thickness of the resist, the exposure dose and the distance between mask and resist.

When the mask and resist are in contact and you expose the resist, you could expect the exposed parts of the resist especially the walls to be perfectly aligned with the mask but due to light diffraction the resist right underneath the mask also gets some exposure and on the micro-scale this has a big effect. The result of diffraction with a positive resist are positively inclined resist walls. The negative resists reaction to this is inverted and both examples can be seen in Figure 3.

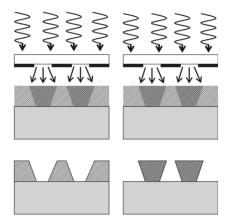


Figure 3: Result of light diffraction during exposure of resist. On the left is the positive resist with exposed parts developed away and on the right is the negative resist with non-exposed parts developed away [1]

Moving the mask further from the resist leads to the light being more diffracted therefore the optimal exposure distance is when there's contact, i.e. no distance. This could either be soft, hard or vacuum contact. With soft contact the wafer was just pressed against the mask. With hard contact the wafer was pushed against the mask using a nitrogen pressure. With the vacuum contact the wafer was sucked against the mask using a vacuuum between the wafer and mask.

Another effect that affects the results is light reflecting and bouncing around inbetween the wafer surface and mask surface. To counteract this the side of the mask that is pointed down toward the resist is coated with an anti-reflecting coating.

#### 2.3.1 TRAVKA 50 Mask

For evaluating the process, a photomask was required that contained a wide range of shapes of different sizes to gain an understanding of how different structures were affected by the process changes. The TRAVKA 50 mask was developed by Danchip staff for this purpose. It features a variety of shapes of different geometries, however, in this investigation, the most interesting were  $2\,\mu{\rm m}$  and  $4\,\mu{\rm m}$  lines as well as  $2\,\mu{\rm m}$  and  $4\,\mu{\rm m}$  triplets. The  $2\,\mu{\rm m}$  structures, as viewed on the mask are shown in Figure 4.

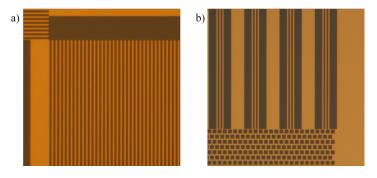


Figure 4: TRAVKA 50 photomask, a) 2 μm lines, b) 2 μm triplets

#### 2.4 Development

Before the wafer goes through development it usually goes through a post-exposure bake which helps the exposed parts of the resist to react as intended. For example with the negative resist the exposed parts cross-link making in harder to develop away so to make sure it cross-links properly it goes through a post-exposure bake allowing the chemical bonds to form. During development, the soluble parts of the resist are dissolved. In the case of positive resists, the developer will dissolve any resist that has been exposed during exposure, as the exposure turns the resist into carboxylic acid. In the case of a negative resist, all but the exposed parts of the resist are etched away because only the parts with exposure have crosslinked.

Developing for too long or too short a time produced visible defects as well. In theory the resist that's resistant should be 100% imumne to the developer. In reality this is sadly not the case, it is etches much slower but still at a rate that's observable if you over-develop the resist. This manifests in positive resists as reduced size of structures and bigger holes, this phenomena is called Dark erosion. Too little development time makes the developer not etch all the way through the resist, which is an essential error, it is, however, often possible to just develop once again to remove the remaining resist.

# 3 Experimental Setup

All machines used are located within the DTU Danchip cleanroom in building 347.

#### 3.1 Spin-coater

For applying the photosensitive resist to the wafer, a Gamma UV spin coater from Suss Microtech was used. We mostly used the same recipe each time which coated a 1.5  $\mu$ m layer of AZ MIR 701 photoresist on the wafer soft-baking it at 90°C for 60s at a distance. In one case, the Gamma UV e-beam spin coater had to be used, however, the same recipe was used as with the Gamma UV.

On this machine it was possible to change the resist thickness and resist type, soft bake time and whether the soft bake should be proximity or contact.

#### 3.2 Aligner

For alignment of the photomask and subsequent exposure, two pieces of equipment were used. Both were MA6 aligners from Suss Microtech, however, one was considerably older than the other. The newer aligner was known as MA6-2 and the older one, KS.

On both machines it was possible to change the distance between wafer and mask, the exposure time and exposure intensity and the exposure mode; proximity, soft contact, hard contact or vacuum contact.

#### 3.3 Developer

After exposing the substrate, development was done in a Suss Microtech developer with the TMAH developer solution.

Here it was possible to change the post-exposure bake, the type of developer and the development time.

#### 3.4 Optical Microscope

For quick and easy inspection of developed wafers, Nikon L200N optical microscopes were used. These offer up to 100x magnification and computer software, allowing for high resolution imaging of the smallest structures on our wafers. Such microscopes also were used to select the area of the wafer to cleave for analysis in a scanning electron microscope.

#### 3.5 Gold Sputter Coater

After selecting an area for further analysis using the optical microscope, the wafer in question must be primed by depositing a thin layer of gold on the surface to lead the electrons from the SEM away from the surface.

#### 3.6 Scanning Electron Microscope

Once coated in gold, the wafer can be cleaved. This involves using a diamond to scratch the surface of the wafer. By applying light pressure, the wafer can then be snapped in two, the cut is straight and clean due to the uniformity of the crystal lattice structure making up the silicon wafer.

# 4 Experimental Work

Over the three week period, five batches of wafers were processed, each made with slight variations in the process in an attempt to remove the problems found in the previous batch.

#### 4.1 General procedure

First the wafer was placed in the spin-coater to prime it for a layer of resist which was deposited after and the type of resist was the same each time. Then this was soft-baked to dissolve the remaining solvent. Hereafter the wafer was placed in the aligner with the same mask each time and exposed. The exposure dose varied between 3 doses. Then the wafer was placed in the developer and got a post-exposure bake. After this it was developed with the same developer and development time where both stayed the same for each batch. When this was finished the wafer was analyzed. Firstly the optical microscope was used to find spots on the wafer shown in Figure 5 worth checking out in the SEM. Then the wafer was coated in gold and cleaved to look at the specific spots. When in the SEM there were measurements taken of each of the chosen spots to get an angle on the sidewalls and give an idea of how good the print was.

# TRAVKA50 layout

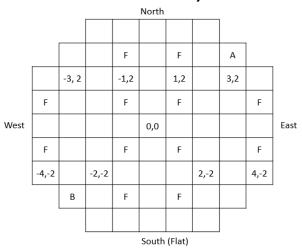


Figure 5: Coordinates of wafer showing the spots that were looked at each time to give an idea of how the print went

#### 4.2 Batch One

Batch one of wafers was coated in silicon dioxide before the course began. The two wafers in the batch were exposed in the aligner for a different length of time - 21s and 32s - to investigate if exposure time affected the sidewall profile.

After developing, both wafers were examined in an optical microscope. Images were taken at different points on the wafer, one particularly interesting point is shown in Figure 6.

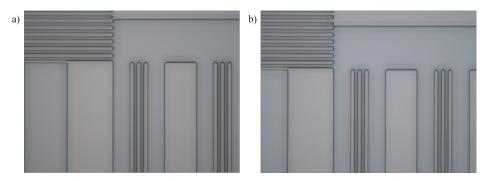


Figure 6: Batch one wafers at different exposures, a) 21s, b) 32s

From these images, it was concluded that increasing the exposure time lead to increased rounding on the ends of the structures and also resulted in a decrease in the critical dimension - in this case, the distance between the structures. A 21s exposure better reflected the shape of the mask.

A suitable location on each wafer was selected for cleaving and viewing in the scanning electron microscope. The images taken are shown in Figure 7.

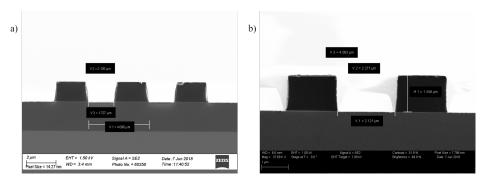


Figure 7: SEM images of batch one wafers at different exposures, a) 21s, b) 32s

From this it can be seen that 32s exposure offers a significantly reduced sidewall angle compared to 21s exposure. However, 32s also showed concave sidewalls on the smallest structures, much unlike the convex edges on the 21s. This suggests that 32s exposure is too long and 21s is possible too short. Therefore, a selection of times between 21s and 32s would likely yield an optimal result. The uneven, light grey coating on the side walls is most likely a layer of gold deposited during sputter coating in larger quantities than usual.

#### 4.3 Batch Two

Batch two contained the first wafers processed during the course, the wafers were coated in resist at the same time as batch one. It was observed that, after development, macroscopic adhesion failure was present on the smaller structures.

Working on advice from the Danchip staff, it was expected that the adhesion failure was due to the age of the coated wafers. When resist costed wafers are left for a length of time, water can absorb into the resist film, hydrating the connection between the substrate and resist, making it less adhesive.

To combat this issue, a fresh batch of wafers was coated ready for processing immediately after.

This new batch was exposed and developed in exactly the same way as initially. On observing the results post developing, it could be seen that there was no visible macroscopic adhesion failure.

Further analysis of each sample was conducted with the aid of an optical microscope. Images were captured for comparison and, as can be seen from the images in Figure 8, the smallest  $1 \,\mu\mathrm{m}$  structures remained intact during the development.

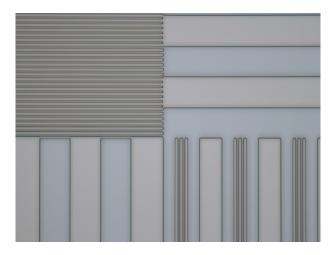


Figure 8:  $2 \mu m$  lines and triplets in batch two, 21s exposure

From this test, we could reliably conclude that for correct adhesion wafers must be coated in resist near the time when they are to be processed. If a longer time is needed between coating and processing, they should be stored in a low humidity environment for a maximum of a few weeks, or else the wafers could become moist and affect structure adhesion.

As previously, a suitable location on the wafer was selected for further analysis under a scanning electron microscope (SEM). This revealed large positive sidewalls, measured at 4° for 21s exposure and 8° for 28s exposure. As can be seen from the SEM image in Figure 9, undercutting near the base of the structure was clearly visible.

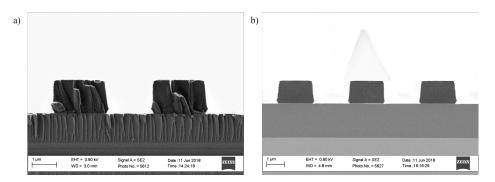


Figure 9: SEM image of  $2 \mu m$  lines on a) 21s exposure and b) 28s exposure

Unfortunately, the 21s wafer was cleaved poorly, however, the overall outline of the structure is still mostly undamaged.

#### 4.4 Batch Three

The third batch of wafers were coated the 8/6 and we exposed and developed on the 12/6. We saw serious adhesion failure which was possibly due to the resist in the maschine being old. The defects seen in the pictures is possibly the result of violent stretching and contracting of the resist surface, making the lines look like snapped strings.

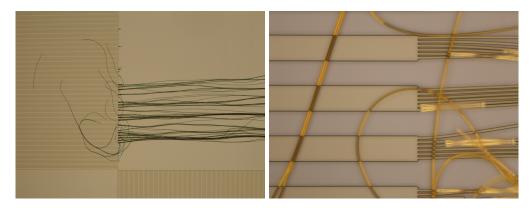


Figure 10: "Hair" defect and "spaghetti" defect

Wafers from the second run in batch two were dehydrated overnight to drive out any moisture before processing the following day.

#### 4.5 Batch Four

The now dehydrated wafers were exposed and developed in the same way as before, this time for 24s, 28s and 32s. After developing, it became apparent that there was significant adhesion failure on almost all  $2\,\mu\mathrm{m}$  lines near then centre on every wafer. Figure 14 shows this adhesion failure near the centre of the wafer.

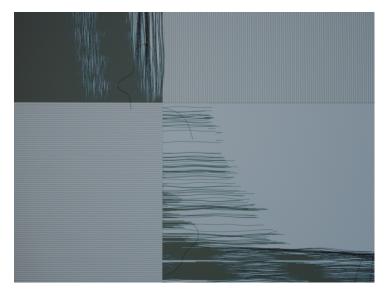


Figure 11: Macroscopic adhesion failure near centre of 24s exposure

This lead us to believe that even with dehydration, the resist was still not able to adhere to the substrate during development with older wafers. To combat this issue, a fresh batch of wafers was coated. This time, silicon wafers were used without an oxide layer, it was thought the oxide layer could be contributing to the adhesion failure seen.

The new wafers were coated in the same way as previously except using the Gamma UV e-beam spin coater. This change should not affect the result at all as the same recipe and resist was used. Three wafers were developed for 24s, 28s and 32s in hard contact and one was developed using vacuum contact for 32s.

No adhesion problems were observed here, however, significant differences could be seen between the wafers. Figure 12 shows the comparison between the aforementioned wafers.

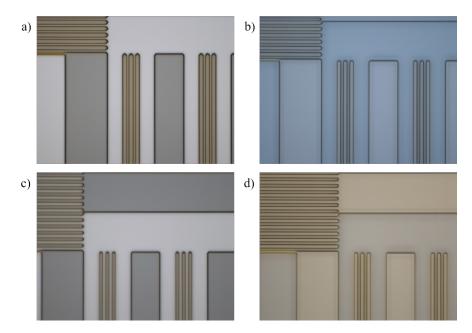


Figure 12: Comparison of  $2\,\mu\mathrm{m}$  lines on each wafer in batch four, a) 24s, b) 28s, c) 32s, d) 32s vacuum contact

Selected locations were sputter coated and cleaved ready for further investigation under the scanning electron microscope.

#### 4.6 Batch Five

In a last effort to counter to undercut problems, we made a batch with 4 wafers to investigate if we would get any improvements by changing the soft baking procedure from proximity bake to contact bake, while testing two different aligners and keeping the exposure time at 28s for all and comparing the results. Sadly we saw no clear improvements changing the softbake parameters, rather we got some new defects at the top of the structures in addition to the undercuts, when we used the MA6-aligner.

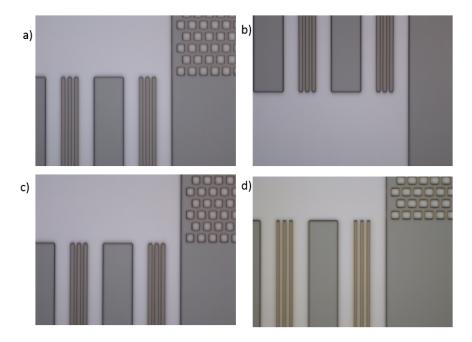


Figure 13: comparison of a) KS proximity bake, b) KS contact bake, c) MA6 proximity bake, d) MA6 contact bake

We see slightly more square structures when using the KS aligner compared to the MA6's rounder edges. However, we see no apparent improvement between proximity and contact bake.

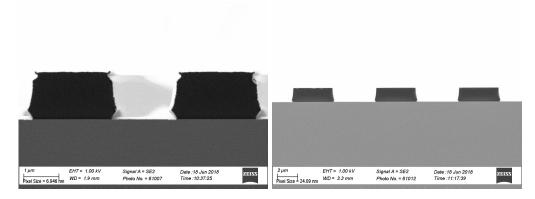


Figure 14: "Shrek"-formation on the MA6-aligner for 28s and still prevalent undercuts when using the KS-aligner

Currently, it is unknown why such defects have formed on the structures. We have communicated with Danchip staff and they also are unsure of what has caused the issues. In an attempt to discover the solution, we have contacted the company manufacturing the resist to see if they have seen similar results before and could shed a light on the issue.

## 5 Future Work

In one instance it was measured that the intensity of the lamp was not what it was programmed to be. This could be one of multiple cases of the equipment not being correctly calibrated. One

next step could be do verify that the equipment is indeed performing as programmed without fault.

Nearer the end of the project, it was brought to our attention that the manufacturer's recommendations for the softbake of the MIR 701 resist had changed from proximity to contact bake. Although our tests showed that proximity and contact bake had very little affect on the result, this is something that could be investigated further.

## 6 Conclusion

From the first run of wafers it was possible to conclude that a set of wafers that had been coated and left in a box in the cleanroom for a couple of weeks would be usable but not for much longer, so the lifetime of these are around a month.

Although the initial aim was not fully met, a great deal of understanding was gained surrounding the processes that will likely help Danchip in the future, both in this problem and in others.

# References

- $[1]\,$  Introduction to Microfabrication, chapter 9 Optical Lithography
- [2] Figure 2 http://slideplayer.com/slide/4936204/#