Hydrogen Annealing for Removal of Scallops after DRIE

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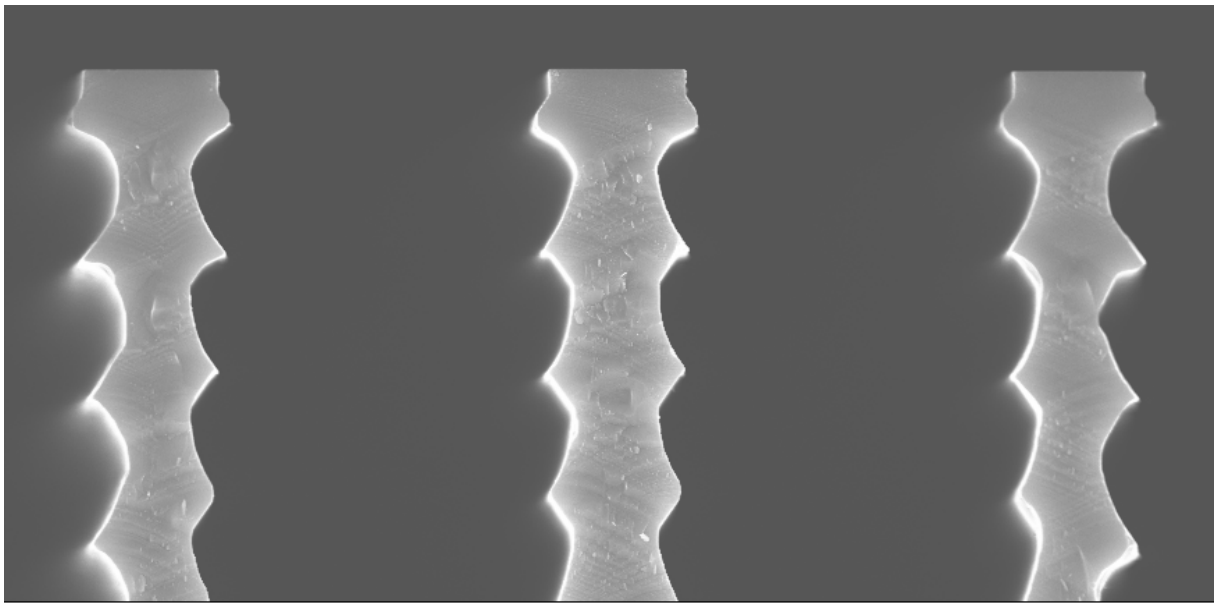


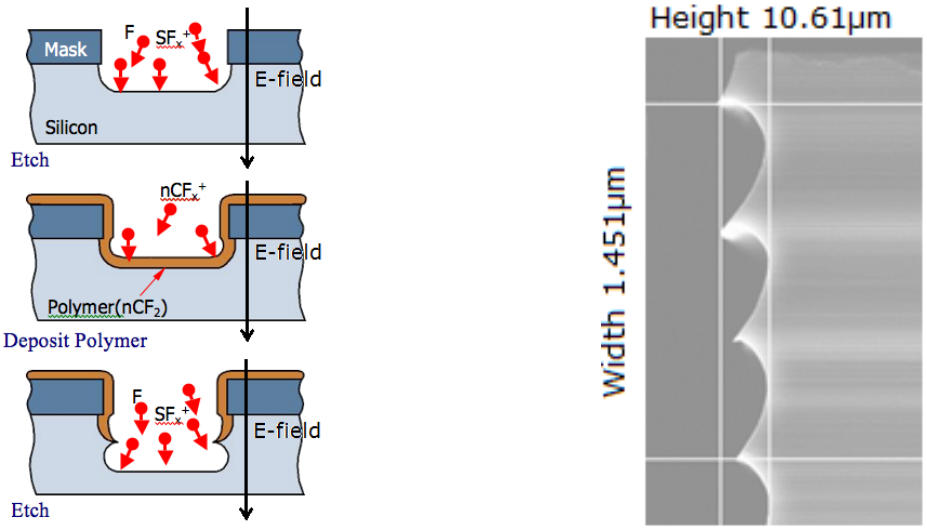
Contents

1 Motivation

When you want to create deep micro channels in silicon you use a technique known as deep reactive ion etching (DRIE). The problem with this technique is that it leaves behind rough sidewalls full of scallops which are undesirable for a.o. optical waveguides and micromirrors [1].
The usual method for getting rid of these scallops is to oxidize the wafer and then remove the oxide using hydrofluoric acid (HF). However, this method is very time consuming, involves HF which is very toxic and the oxidation process consumes some of the silicon thus making it difficult to control the size of the etched structures [2].
Recently another approach for scallop removal has been suggested. The idea is to use hydrogen annealing at high temperatures (>1000 $^{\circ}C$) and low pressure (<0.5 bar). At this temperatures and pressure the mobility of the silicon atoms is increased and the pointy scallops should be smoothed out as the silicon tries to minimize the surface energy.
In our project we have created microstructures of different size using the DRIE process on <100> silicon wafers. The annealing has been done using both hydrogen (H_2) and nitrogen (N_2) in both an ATV-furnace and a CVD furnace (Black Magic) under temperatures ranging from 980 $^{\circ}C$ to 1100 $^{\circ}C$ and pressure ranging from 9 $mbar$ to atmospheric pressure both on RCA cleaned and non-RCA cleaned silicon wafers.
The wafers have been investigated before and after annealing using scanning electron microscopes (SEM) and optical microscopes.

2 DRIE

For the DRIE process - or "Bosch process" - we use wafers with a resist mask to create structures in the wafer (please note that the photo lithography is not a part of our project). The DRIE process (see figure 1a) works by etching the silicon wafer using a plasma etch consisting of SF_6. Then you deposit a passivation layer consisting of a polymer, C_4F_8, and start the plasma etch again. This cycle is repeated over and over until the desired depth has been reached. The etching itself is isotropic, i.e. will attack the silicon evenly in all directions, but by applying an electric field to the etching plasma the directional ions or "radicals" will chip away at the passivation layer mainly in the vertical direction, thus exposing the silicon below to the plasma etch. This ensures that the etching is mainly vertical, but it is not perfect and thus still leaves behind scallops as seen on figure 1b.



(a) (b)

Figure 1: Figure **a**: Illustration of the DRIE process. Though the etch is isotropic the directional E-field makes sure the radicals chip away at the passivation layer mainly in the vertical direction (modified from `https://www.mems-exchange.org/images/about_mems/drie.png`). Figure **b**: SEM image of the scallops developed by using DRIE. The specific DRIE process used is "process A" (parameters in figure 2)

The depth of the etched structure depends on the width of the mask and the number of cycles. It also depends on the strength of the E-field applied (the coil and platen power) and time intervals of the etching and depositing respectively. It also depends on the gas flow, the pressure and temperature. To develop the scallops seen on figure 1b we have used the "SPTS DRIE Pegasus", "process A" (parameters in the table 2).

	Process A parameters			
	Step 1		Step 2	
Parameter	Etch	Dep	Etch	Dep
Gas flow (sccm)	SF_6 350 (1.5 s) 550	C_4F_8 200	SF_6 350 (1.5 s) 550	C_4F_8 200
Cycle time (secs)	7.0	4.0	7.0	4.0
Pressure (mtorr)	25 (1.5 s) 90 >> 150	25	25 (1.5 s) 150	25
Coil power (W)	2800	2000	2800	2000
Platen power (W)	120 >> 140 (1.5) 45	0	140 (1.5) 45	0
Cycles	11 (keep fixed)		44 (vary this)	
Common	Temperature 20 degs, HBC 10 torr, Short funnel, with baffle & 5mm spacers			

Figure 2: Process parameters for "process A" on the "SPTS DRIE Pegasus"-machine, [4]
Note: sccm = standard cubic centimeters.

"Process A" gives very consistent structures so that it will be easy to find the same specific reference structure on each of the samples. This makes it easy to compare the different samples with one another once we try to reduce the scallops.

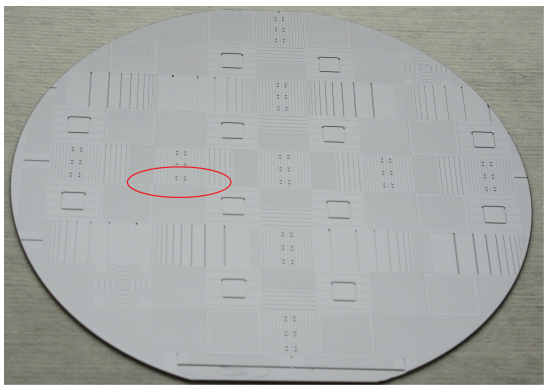


Figure 3: Picture of the etched wafer and the area we are looking at.

3 Annealing Theory

As mentioned earlier, hydrogen annealing is suggested as a promising way to reduce or even remove scallops. When the surface atoms reach temperatures over 800 $^{\circ}C$ the surface starts to become a bit viscous, which allows the silicon surface atoms to move around the surface. An effect of the migration of the surface atoms is that the surface atoms tend to reduce the roughness of the surface because it minimizes the total surface energy without reducing the volume.This basically means that the sharp corners the scallops have should be less sharp or even disappear after hydrogen annealing.

The diffusion of the silicon atoms depends on the temperature and the pressure. Increasing the temperature increases the diffusion, however there is a upper limit at around 1400 $^{\circ}C$, which is the melting point of silicon. Hydrogen annealing of silicon to reduce surface roughness tends to be done at low pressure. The reason is that increasing the pressure suppresses the migration of the silicon atoms. One of the reasons why one uses hydrogen when annealing is because the heated hydrogen enhances the mobility of the surface atoms [1].

In this paper, we will try various combinations of temperature, pressure, annealing time and gas under annealing hydrogen or nitrogen. We will try to investigate how big an impact the different parameters have on the reduction of scallops and which specific parameters that reduces the scallops most.

To heat our samples to the desired temperature, we used the cleanroom's ATV PEO-604 furnace and Black Magic. The ATV furnace can heat up to 1100 $^{\circ}C$. Furthermore, the furnace can also alter the pressure inside the furnace. The furnace operates at either atmospheric pressure or vacuum ($0.1mbar$). The ATV furnace gives us the possibilities to do annealing around 1100 $^{\circ}C$ at $1atm$ with either hydrogen or nitrogen. However, due to an interlog in the software of the furnace, one can not heat the furnace above 1000 $^{\circ}C$ in vacuum. Fortunately, the Black Magic furnace can do annealing at 1100 $^{\circ}C$ in vacuum while pumping hydrogen or nitrogen.

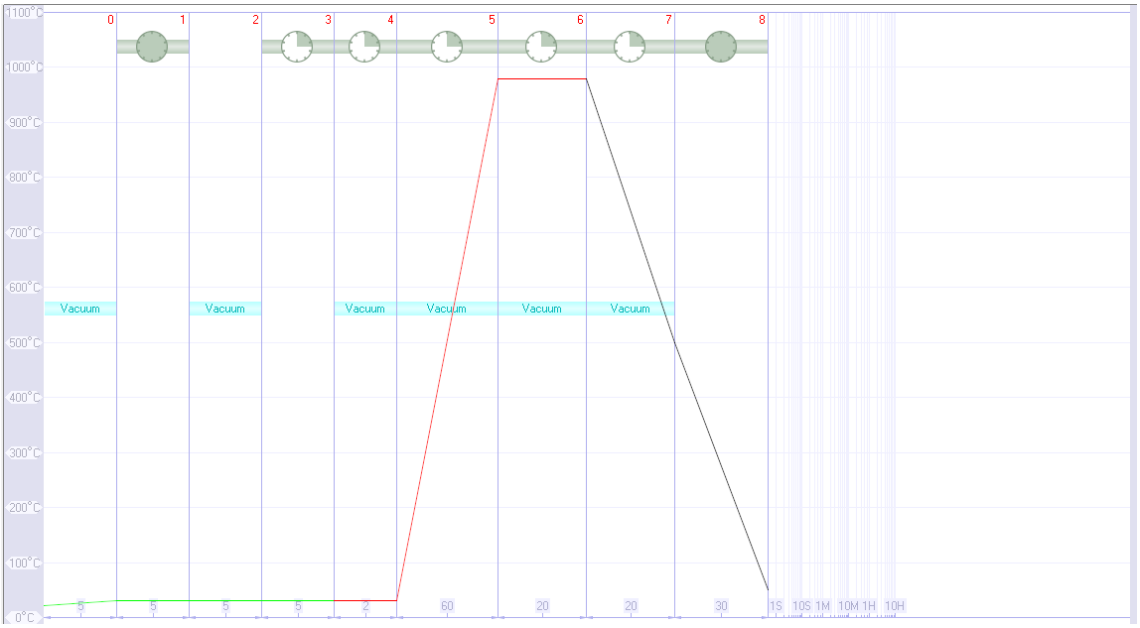
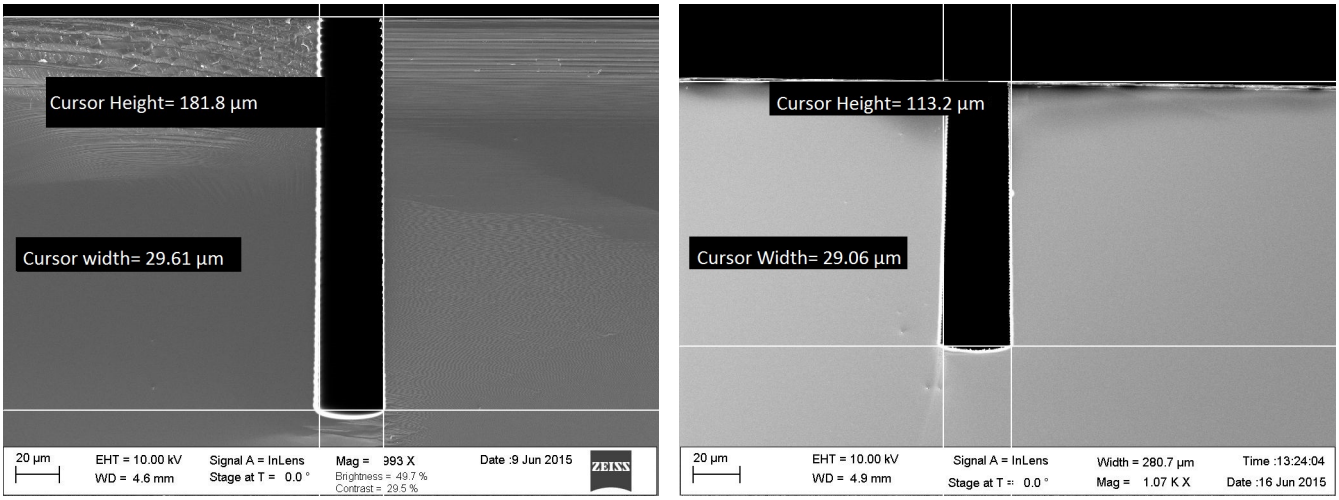


Figure 4: The recipe for the sample, which is going to be annealed in nitrogen at 980 $^{\circ}C$ for 20 min, in vacuum. The green line shows the temperature during the pump/purge cycle, the red one shows the temperature when heating, and the black one shows the temperature during cooling. The green bar with the clock indicates when nitrogen was present and with what flow.The light blue bar indicates periods with vacuum. A recipe for 1100 $^{\circ}C$ at 13 mbar for 5 minutes for Black Magic is shown in appendix B

As seen in figure 4 we start by pumping with vacuum for 5 minutes followed by a 5 minutes purging with nitrogen. The reason why we do a pump/purging cycle is to dilute the concentration of oxygen, since oxygen can make a reaction with the silicon and create silicon oxide ($Si0_2$), which we are not interested in. We do two cycles of pump/purging with nitrogen to make sure that the concentration of oxygen is low. After the pump/purging cycles we do another pumping in vacuum for 5 minutes while purging with nitrogen before heating the sample. The sample is then heated from 50 $^{\circ}C$ to 980 $^{\circ}C$ in 1 hour in vacuum while pumping with nitrogen. When the furnace reaches 980$^{\circ}C$ the annealing process takes place. In this experiment, the annealing time is 20 minutes in vacuum while pumping nitrogen. After the 20 minutes of annealing at 980 $^{\circ}C$ the furnace cools down to 500 $^{\circ}C$ still under vacuum. This cooling takes about 1 hour. The last part of the cooling is done without vacuum.

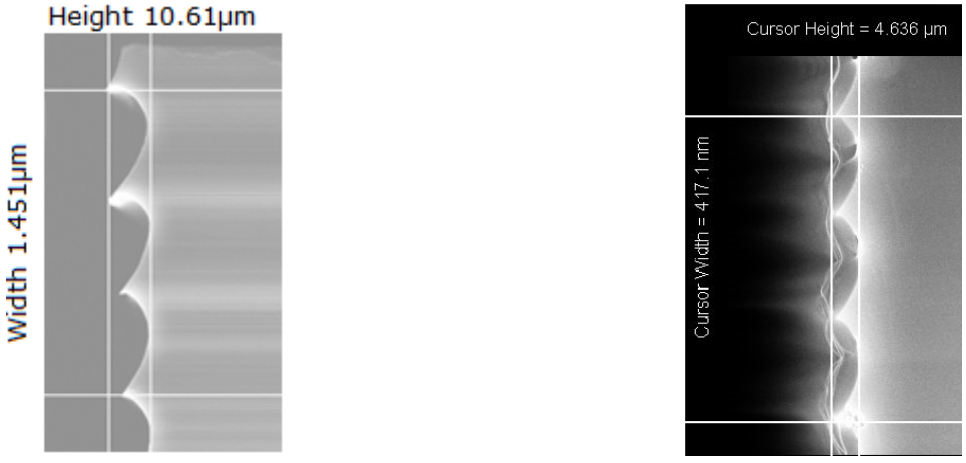
4 Experiments

To compare the results from the different samples (see table 1-3), we first had to choose a trench reference structure. The main reference structure we chose (sample 6) was 181.8 μm deep and 29.6 μm wide (see figure 5a). The scallops were about 1.0 wide and the distance between each scallop tip was around 3.5 μm. This specific reference structure was what we looked for on each of the samples up until sample 16.
At this point we ran out of etched wafers and had to make some new ones. These new wafers were created on the SPTS DRIE Pegasus using the "Henri process" (parameters in appendix A) and thus have different depth, width and scallop size. The mask used was the same as for the first wafers. The depth of the new reference structure (sample 14) was 113.2 μm and the width was 29.1 μm (see figure 5b). The scallops were about 417.1 nm wide and the distance between each scallop tip was around 1.5 μm. This reference structure was used for the remainder of the samples (sample 17-22).



(a) (b)

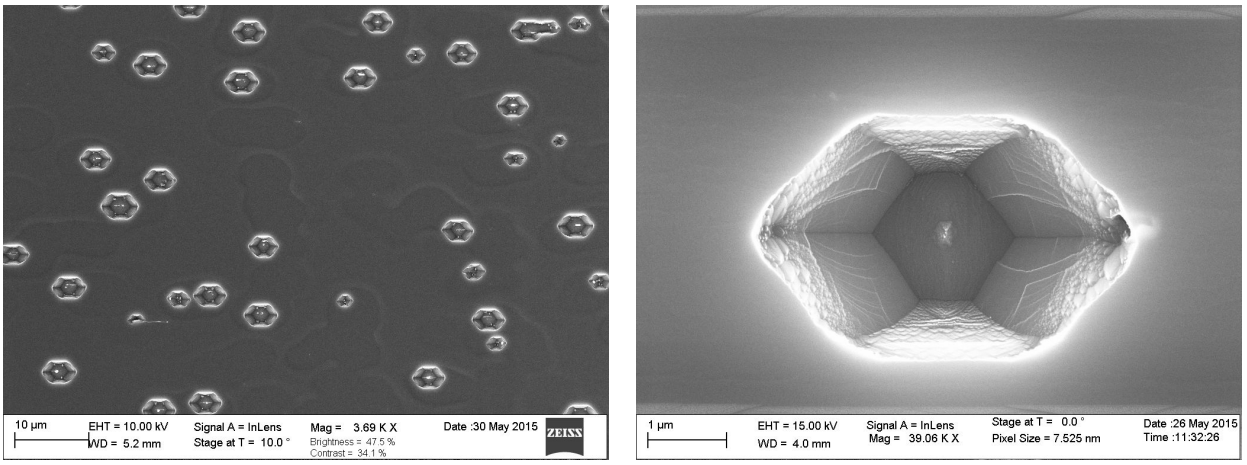
Figure 5: Figure **a**: sample 6: Main reference structure made by "process A". Figure **b**: sample 14: Secondary reference structure made by "Henri process".



(a) (b)

Figure 6: Figure **a**: sample 0: close-up of the scallops in the main reference structure made by "process A". Figure **b**: sample 14: close-up of the scallops in the secondary reference structure made by "Henri process".

We tried multiple approaches to anneal the scallops. Sample 0-5 was made by our tutors Pernille Voss Larsen and Mikkel Dysseholm Mar. They annealed with H_2 under a pressure of 1 atm and temperatures ranging from 1050 °C to 1100 °C. Their results suggested impurities in the process since it was found that the surface appeared to be etched during the annealing process (see picture 7a and 7b). Hence they tried annealing wafers that had just been dipped in buffered HF to get rid of any naturally occurring oxide, and even tried to change the quartz tube of the oven, to no avail (see table 1).

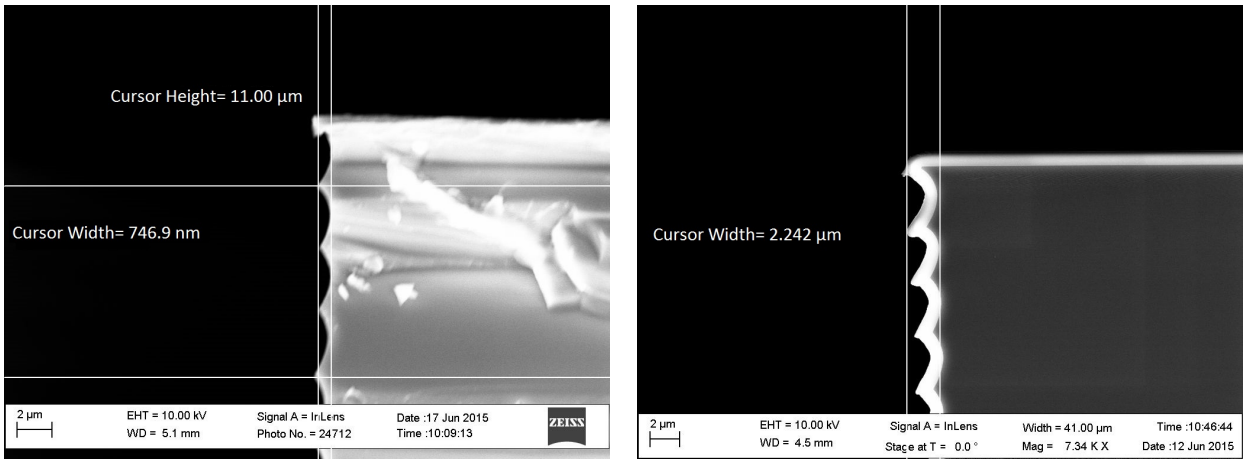


(a) (b)

Figure 7: Figure **a**: Edge (<110> plane) of sample 2 showing hexagonal etches. The etching stops along the <111> plane. Figure **b**: close-up of the hexagonal etch on the surface.

The experiments on sample 7-9 we conducted ourselves. Here we tried annealing with H_2 at 1100 °C under a pressure of 1 atm, varying the time from 20 min to 40 min. We also tried annealing with N_2 instead. We did not see any scallop reduction but the surface of sample 9 appeared to be etched at the edges. It was suggested that this etching was due to impurities on the wafers. We conducted an energy-dispersive X-ray spectroscopy (EDX-analysis) of the surface of sample 9, but found only silicon.
On sample 10 and 11 (see figure 8a and 8b) we tried scallop reduction by wet oxidation in a furnace tube with H_2O-vapour. When you oxidize silicon, you create a layer of SiO_2 on the surface, which is then removed using HF. The oxidation layer thickness depends on the time and temperature of the oxidation (see appendix C). We grew 1 µm of oxide at 1 atm pressure and 1050 °C for 3 h 20 min. Since there goes two molecules of oxygen to each molecule of silicon, we expect to have removed about 0.3 µm of the silicon. As expected, about 1/3 of the silicon was removed, so the scallops were reduced by about 1/3, but at the cost of a widening of the structure as a whole.

Sample 17-20 (see figures 9a, 9b, 10a, 10b) were first RCA-cleaned to get rid of impurities on the wafer and then transferred to the "Black Magic" CVD-furnace using clean gloves and a clean box. Here they were annealed with H_2 under a pressure of 13 mbar. The temperature was varied from 1050 °C to 1100 °C and the time from 5 min to 20 min.
On sample 17 which was annealed at 1050 °C for 20 min we saw a clear scallop reduction. However the surface had been roughed up.
On sample 18 which was annealed at 1100 °C for 10 min we might have seen a minor scallop reduction, but it was not enough to be significant. The surface appeared etched/damaged, more than sample 17.
On sample 19 which was annealed at 1100 °C for 5 min we saw no scallop reduction. The surface appeared a little etched/damaged, but not as much as sample 18.
On sample 20 which was annealed at 1050 °C for 10 min we saw a minor scallop reduction. The surface was very damaged about the same as sample 17.
It was suggested that the destruction of the surfaces could be due to all the copper present in the CVD furnace since the wafers themselves were clean. The copper leftovers were there because the oven is usually used for other purposes, mostly graphene. To check for copper on the wafers after the annealing, we conducted an



(a) (b)

Figure 8: Figure **a**: sample 10: measurement of scallops *after* oxide removal with HF. Figure **b**: sample 11: measurement of scallops and oxide *before* oxide removal with HF

EDX-analysis of the wafers but found no trace of copper, only silicon was found.
Sample 21 (see figure 11a) was also RCA-cleaned. Then it was annealed in the ATV furnace with N_2 for 20 min at 1100 $°C$ under atmospheric pressure. There might have been a minor scallop reduction but the results were inconclusive. The surface was smooth which suggests that we got rid of the impurities. The "nano-grass" structures seen are due to a failure in the etching process in the SPTS Pegasus.
Sample 22 was RCA-cleaned as well and then dipped in HF just before the annealing with N_2 in the ATV furnace at 980 $°C$ for 20 min under a pressure of 9 mbar. We saw no scallop reduction, and we saw only a minor etch of the surface and only around the etched structures (see figure 12b).

5 Results

Table 1: Samples 0 to 6

Sample number	0	1	2	3	4	5	6
Date	28-05-2015	08-06-2015	28-052015	01-06-2015	01-06-2015	02-06-2015	08-06-2015
Sample	Travka05	Cleaved Si wafer	Cleaved Si wafer	Cleaved Si wafer	Travka05	Travka05	Travka05
RCA Clean		No	No	No	No	No	
HF etch		No	Bhf	No	No	No	
Annealing Temperature [$°C$]		1100	1100	1100	1100	1050	
H2 annealing Time [min]		20	20	20	20	20	
N2 annealing Time [min]		0	0	0	0	0	
Gas ramp up temp		H2	H2	H2	H2	H2	
Gas ramp down temp		H2	H2	H2	H2	No	
Furnace tube Comment	Reference	Pyrolysis	Pyrolysis	Clean	Clean	Clean	Reference
Scallop reduction		No	No	No	No	No	
Surfaces comment		etched	etched	etched	etched	etched	

Table 2: Samples 7 to 12 and 16

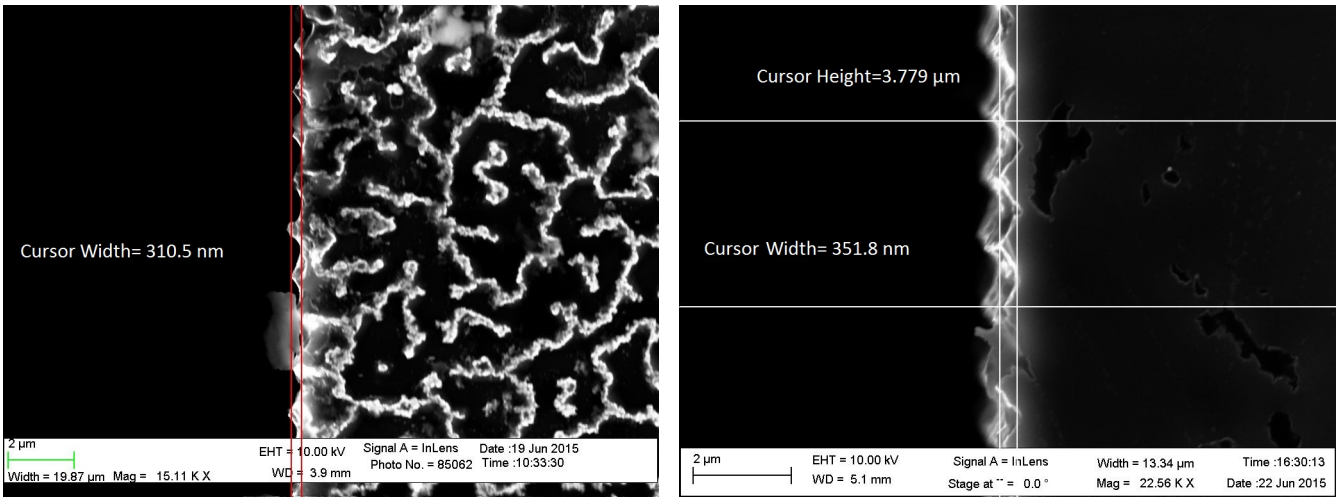
Sample number	7	8	9	10	11	12	16
Date	08-06-2015	08-06-2015	08-06-2015	09-06-2015	11-06-2015	11-06-2015	11-06-2015
Sample	Travka05	Travka05	Travka05	Travka05	Travka05	Travka05	Travka05
RCA Clean	No	No	No	Yes	Yes	Yes	Yes
HF etch	No	No	No	Yes	Yes	Yes	Yes
Annealing Temperature [$^{\circ}C$]	1100	1100	1100	1050	1050	1100	980-998
H2 annealing Time [min]	20	0	40	0	0	0	0
N2 annealing Time [min]	0	20	0	20	20	20	20
Gas ramp up temp	N2	N2	N2	N2	N2		N2
Gas ramp down temp	N2	N2	N2	N2	N2		N2
Furnace tube	Pyrolysis	Pyrolysis	Pyrolysis	A1	A1	C3	Pyrolysis
Comment				Oxidation	Oxidation		Failed
Scallop reduction	No	No	No	Yes	Yes	No	No
Surface comment	etched	etched	etched	Smooth	Smooth Still oxide pressence	etched	

Table 3: samples 17 to 22 and 14

Sample number	14	17	18	19	20	21	22
Date	16-06-2015	18-06-2015	18-06-2015	19-06-2015	19-06-2015	18-06-2015	19-06-2015
Sample	Travka05	Travka05	Travka05	Travka05	Travka05	Travka05	Travka05
RCA Clean	Yes	Yes	Yes	Yes	Yes	Yes	Yes
HF etch	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Annealing Temperature [$^{\circ}C$]		1050	1100	1100	1050	1100	980
H2 annealing Time [min]		20	10	5	10	20	0
N2 annealing Time [min]		0	0	0	0	0	20
Gas ramp up temp		Ar	Ar	Ar	Ar	N2	N2
Gas ramp down temp		Ar	Ar	Ar	Ar	N2	N2
Furnace tube		BM	BM	BM	BM	Pyrolysis	Pyrolysis
Comment	Reference	Just RCA Cleaned				Just RCA Cleaned	Just HF Dipped
Scallop reduction		Yes	Incon-clusive	No	minor	Incon-clusive	No
Surface comment		etched damaged	etched damaged	etched damaged	etched damaged	smooth nano grass	smooth

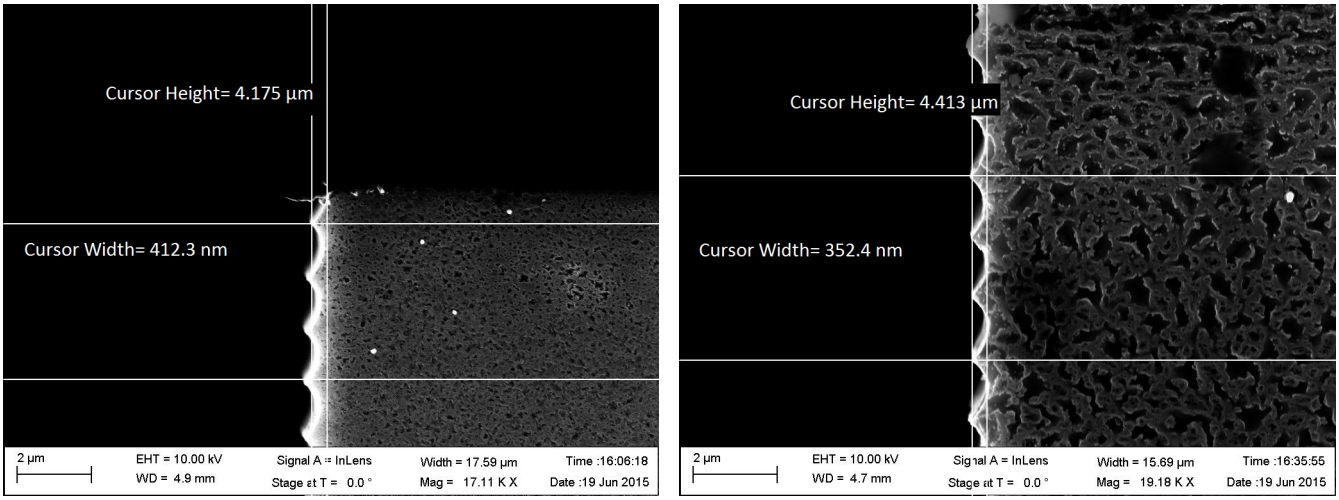
Comments:
A1 = Boron Drive-in + Pre-dep furnace.
C3 = Anneal-bond furnace.

BM = Black Magic CVD furnace.
Samples 13 and 15 were dummy wafers.



(a) (b)

Figure 9: Figure **a**: Scallop measurement of sample 17 which has been annealed in the Black Magic furnace for 20 min with H_2 at 1050 $°C$ and 13 $mbar$. Figure **b**: Scallop measurement of sample 18 which has been annealed in the Black Magic furnace for 10 min with H_2 at 1100 $°C$ and 13 $mbar$.

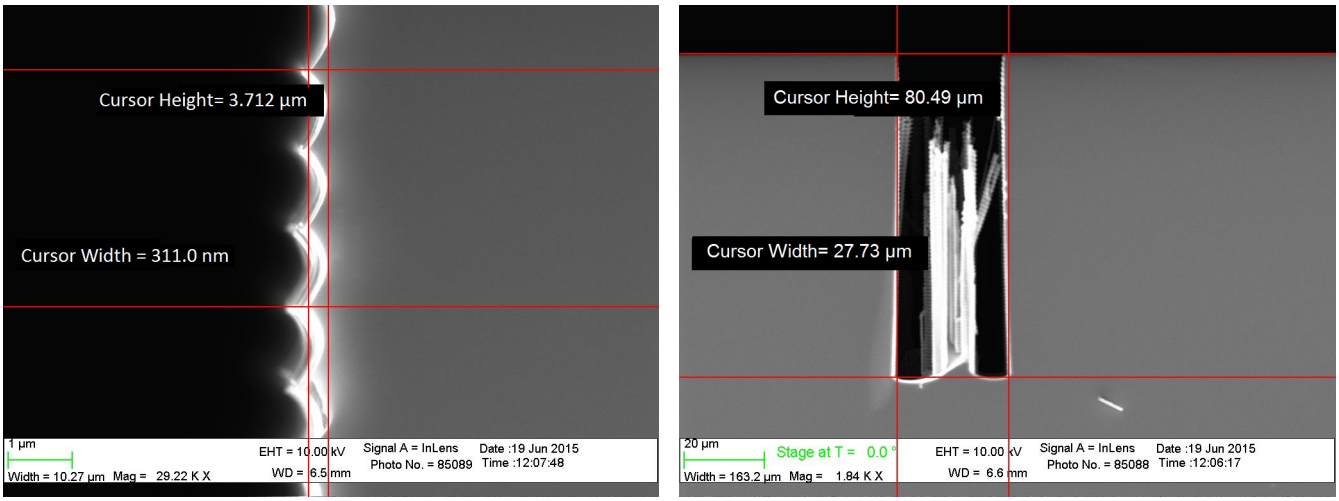


(a) (b)

Figure 10: Figure **a**: Scallop measurement of sample 19 which has been annealed in the Black Magic furnace for 5 min with H_2 at 1100$°C$ and 13 $mbar$. Figure **b**: Scallop measurement of sample 20 which has been annealed in the Black Magic furnace for 10 min with H_2 at 1050$°C$ and 13 $mbar$.

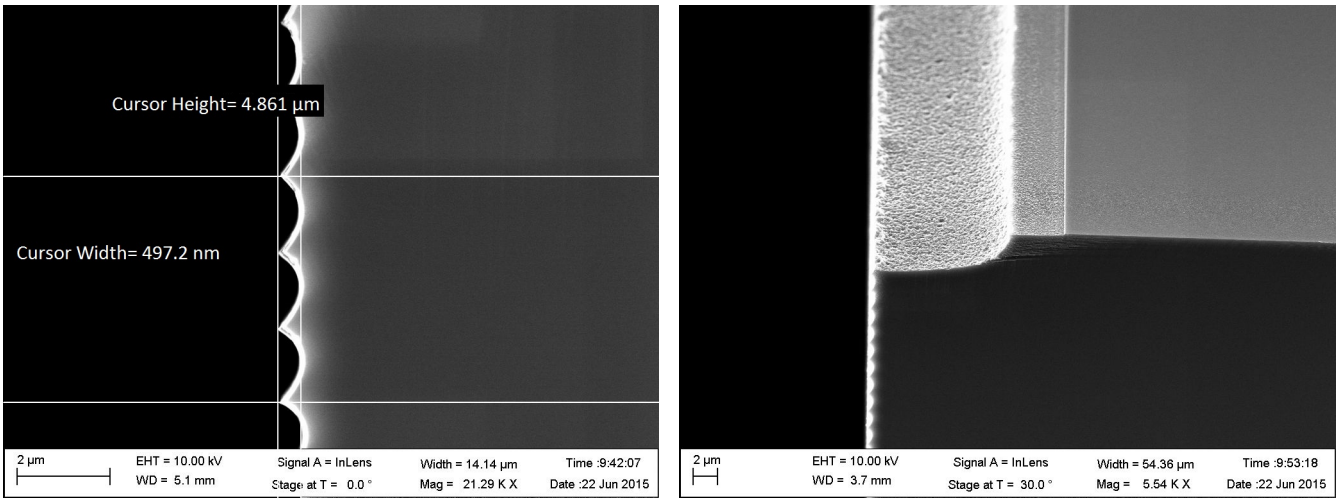
6 Discussion

Looking at the first 5 wafers (sample 1-5) we saw no scallop reduction. We think this is due to the pressure at 1 atm being too high. The etching of the surface that we see, we think is due to impurities on the wafer, maybe obtained from the Pegasus etch or from resist leftovers since we did not put the wafers in the plasma asher (it cant be in the oven since we changed the quartz furnace tube). We know that hydrogen at high temperatures



(a) (b)

Figure 11: Figure **a**: Scallop measurement of sample 21 which has been annealed in the ATV furnace for 20 min with H_2 at 1100 $^\circ C$ and 1 atm. Figure **b**: Overview of sample 21 with the nano grass present



(a) (b)

Figure 12: Figure **a**: Scallop measurement of sample 22 which has been annealed in the ATV furnace for 20 min with N_2 at 980 $^\circ C$ at 9 $mbar$. Figure **b**: front of sample 22 showing how the roughness is greater at the edges of the etched structures.

and high pressure has etching properties, but need some sort of catalyst to start the process of making silane ($Si + 2H_2 \rightleftharpoons SiH_4$)[5].

Regarding samples 7-9 we saw no reduction of scallops. We think that this is again due to the high pressure of 1 atm. and that N_2 in general does not work as an annealing agent. Looking at the wafer from sample 9, we saw that the etching of the surface was most severe at the edges. Why this is, we do not know but it is possible that the gas flow around the wafer has resulted in some edge-effects. The pyramidal etching of the surface we still think is due to impurities. The etch is pyramidal because the bonds in silicon are denser along the <111> plane.

Oxidation is a way to reduce scalloping as seen from sample 10 and 11, but it will consume some of the silicon and therefore is not viable when the structures are very small (< 3 ţm).

Sample 12 was a repetition of the N_2 annealing but in another furnace with a wafer that had just been RCA-cleaned. Nothing happened which suggests that N_2 is neither an etching agent nor an annealing agent.

Sample 16 has seen multiple interrupted attempts at annealing with hydrogen at temperatures above 1000 $^\circ C$ which always failed at 998 $^\circ C$. At last we tried N_2 at 980 $^\circ C$ at 9 $mbar$ but still saw no scalloping reduction which again suggests that N_2 is not an annealing agent. The surface was damaged though it never saw any H_2 and the wafer was RCA-cleaned prior to annealing, but due to all it has been exposed to, we cannot conclude anything.

Sample 17 had just been RCA-cleaned before it was annealed in the Black Magic furnace. Here we saw scallop reduction but the surface was damaged. We think the damaging of the surface is due to all the copper that was in the furnace chamber, suggesting that Cu can act as a catalyst for the hydrogen etching process. However we did not see the characteristic pyramidal structures which may be due to the short annealing time or the low pressure or that the wafer had just been cleaned.
Sample 18 had also been RCA cleaned. The scallop reduction was not large enough that we were able to definitely conclude anything. The surface was damaged, but did not have the pyramidal structures. We think the lack of scallop reduction and development of structures may be due to the shorter annealing time.
Sample 19 had no visible scallop reduction, but we think this is due to the short annealing time. The surface is not as damaged either, which we also think is due to the short annealing time.
Sample 20 had some minor scallop reduction though it was annealed at a lower temperature but the same amount of time as sample 18. We saw clear pyramidal structures on the surface. This suggests that annealing at 1050 $^\circ C$ is more effective than annealing at 1100 $^\circ C$, contrary to the literature [1]. Further testing - preferably in a cleaner furnace tube - needs to be done to fully determine this.

Sample 21 had just been RCA-cleaned and was annealed in the ATV furnace at 1100 $^\circ C$ for 20 min under 1 $atm.$ pressure. We were not able to determine whether or not the scallops actually had been reduced, but the surface was very smooth compared to its predecessors. This indicates that a clean furnace tube and clean wafer stops the H_2 from etching since there are no catalysts present. The nano grass is due to a failure during the DRIE process. Sample 22 had just been HF dipped and was annealed with N_2 at 980 $^\circ C$ at 9 mbar. We saw no scallop reduction and hardly any surface damage, which indicates that N_2 is neither an annealing nor an etching agent. We did see some damage on the surface around the edges of the structures, but we think this may be due to the photo lithography (the surface at the edges of the structures are more ruined the smaller the structure becomes).

The EDX-analysis of sample 9, 19, and 20 showed no sign of any impurities on the surface, but this may be due to the weight percentage of the impurities not being high enough i.e. higher than 1 $Wt\%$.
It has been suggested that the oxygen levels in the furnace has not been low enough and that this may be the cause of the surface damage. We know that the oxygen will react with the silicon creating SiO_2 and that even a small amount of oxygen can do some damage. Ideally our O_2-concentration should be around $1 \times 10^{-7}\%$ after the pump-purge cycles, but to be certain, we might want to run more pump-purge cycles before we start the annealing process in a future experiment.

7 Conclusion

We can conclude that it is very important to clean the wafers prior to annealing to avoid surface etching. We can also conclude that an annealing process using N_2 as reactant/catalyst will not work.
We saw a scallop reduction when we used H_2 and low pressure for the annealing but at the cost of a ruined surface. This could be due to the copper contamination of the furnace but further testing is needed to see if this is true.
Furthermore we can conclude that the pressure has to be low for the H_2 annealing process to work.
We confirmed that oxidation followed by HF removal is a viable way to reduce scalloping but that this will also consume some of the silicon thus widening the structure.

Appendixes

A SPTS Pegasus, "Henri process" parameters

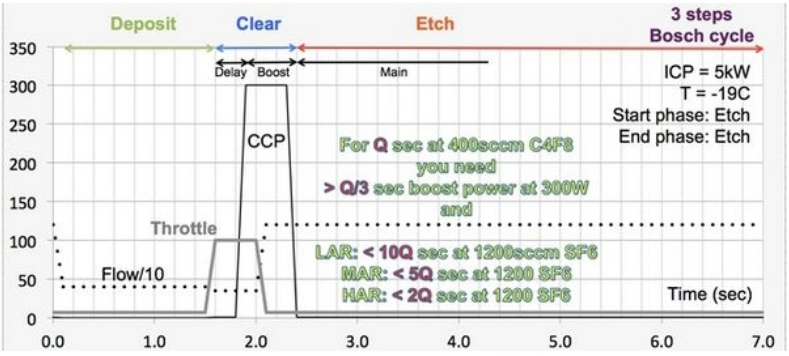
June 2nd 2015

Descum 3s40 sccm O2@15mtorr,200L/20L W, PI:L/T 30/50, D/E auto/auto, 10 s stab

		D	B	M C_4F_8	Delay	Boost	M SF_6	Cycl	MU	
4999L W coil, -19dgC, C4F8/SF6=1/5 sec,ET 5.00, 1s stab, 20 T He	Flow (s/sccm)	-	-	1/400	-	1/350	4/700	50	PI L/T 35a/45a	Profiles of feature -
	Throttle (s/%)	-	-	6.8	-	1/100	-/10	S=E	Coil L/T 30a/55a	
	Platen (s/W)	-	-	-	0.3/1	0.7/100	-/1	E=E		

Observation:

Henri/PP base 2



June18 2015

Descum 3s40 sccm O2@15mtorr,200L/20L W, PI:L/T 30/50, D/E auto/auto, 10 s stab

		D	B	M C_4F_8	Delay	Boost	M SF_6	Cycl	MU	Profiles of feature
4999L W coil, -19dgC, C4F8/SF6=0.5/5 sec,ET 5.00, 1s stab, 20 T He	Flow (s/sccm)	-	-	1/400	-	1/350	4/700	**150**	PI L/T 35a/45a	
	Throttle (s/%)	-	-	6.8	-	1/100	-/10	S=E	Coil L/T 30a/55a	
	Platen (s/W)	-	-	-	0.5/1	0.5/100	-/1	E=E		

Observation: S005603

Henri/PP base 2

June18 2015

Descum 3s40 sccm O2@15mtorr,200L/20L W, PI:L/T 30/50, D/E auto/auto, 10 s stab

		D	B	M C_4F_8	Delay	Boost	M SF_6	Cycl	MU	
4999L W coil, -19dgC, C4F8/SF6=0.5/5 sec,ET 5.00, 1s stab, 20 T He	Flow (s/sccm)	-	-	1/400	-	1/350	4/700	**250**	PI L/T 35a/45a	Profiles of feature -
	Throttle (s/%)	-	-	6.8	-	1/100	-/10	S=E	Coil L/T 30a/55a	
	Platen (s/W)	-	-	-	0.5/1	0.5/100	-/1	E=E		

Observation: S005604

Figure 13: Overview of the parameters in the "Henri process" run in the SPTS Pegasus

B Black magic recipe and data example

The process we ran in the Black Magic oven for sample 19 which was annealed in H_2 at 1100° C at 13 mbar for 5 minutes.

Recipe:

VALV 1 CLOSE
TUNE PCON SWNT at 10mbar
PCON ON 13.0 20.0
WAIT PRES < 20.00
FLOW 2 ON 500
TUNE HTTC 41.0
TUNE TOPH 40.0
TOPH ON 500.0 200.0
HEAT ON 500.0 200.0
WAIT TEMP > 450.0
TUNE TOPH 75.0
TUNE HTTC 75.0
HEAT ON 1100.0 200.0
TOPH ON 1100.0 200.0
WAIT TEMP > 1090.0
FLOW 2 OFF
FLOW 6 ON 1000
WAIT TIME > 300
FLOW 6 OFF
FLOW 1 ON 1000
FLOW 2 ON 1000
HEAT OFF
PCON OFF
TOPH OFF
WAIT TEMP < 350.0
FLOW 2 OFF
FLOW 1 OFF
VALV 1 OPEN
WAIT PRES < 0.10

Data:

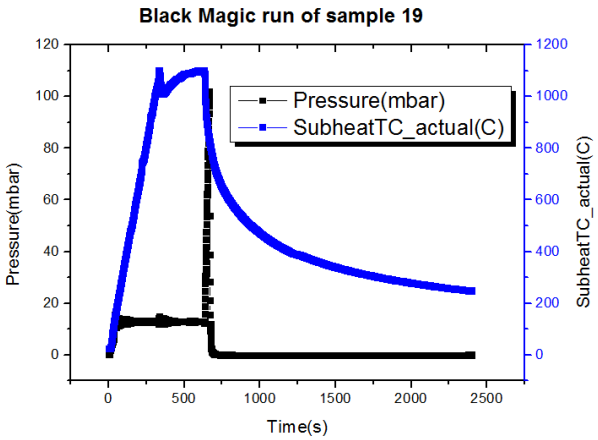


Figure 14: Overview of the Black Magic run for sample 19

C Wet oxide thickness

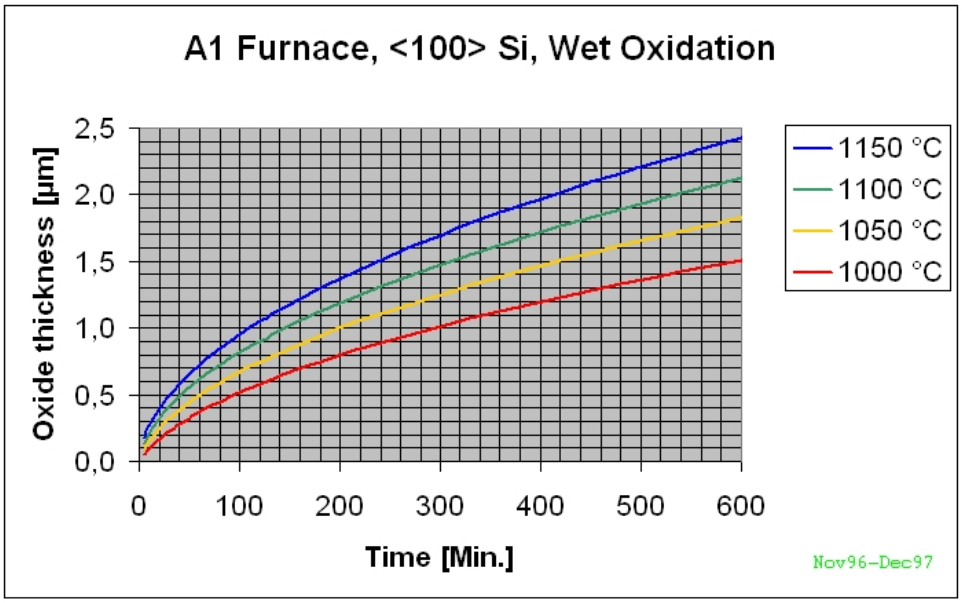


Figure 15: Graph of the wet oxide thickness vs. time for different temperatures for the A1 Boron Drive-in + Pre-dep furnace.
Source: `http://labadviser.danchip.dtu.dk/images/f/fc/A1_furnace_100_Si_wet_oxidation.jpg`

For further information on the furnace see `http://labadviser.danchip.dtu.dk/index.php/Specific_Process_Knowledge/Thermal_Process/A1_Bor_Drive-in_furnace`

References

[1] Ming-Chang M. Lee and Ming C. Wu, Thermal Annealing in Hydrogen for 3-D Profile Transformation on Silicon-on-Insulator and Sidewall Roughness Reduction, Journal of Microelectromechanical Systems vol. 15 no. 2 april 2006.

[2] Pernille Voss Larsen, project description from "Catalogue of 3 week projects at DTU NanoTech".

[3] original picture from `https://www.mems-exchange.org/images/about_mems/drie.png`
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