|  |
| --- |
| Objective |
| Batch name: Process template |
| This process flow is a guideline on how to spin coat, expose, and develop AZ 4562 on 100 mm substrates such as Si, SiO2 and Borofloat, using automatic spin coater, maskless aligner and automatic developer.  This is an example process flow to be used as a template. It should contain:   * The objective of the process * Substrates/samples used in the flow - both actual samples to be processed (device wafers) and any monitor samples for the different process steps * The Process flow main processes and steps * Recommended: Figures illustrating the sample before and after each main process step   How to use this template (works only with the .dotx template file):   * Fill out the fields in the header * Add process steps by using Quick Parts under Insert (your cursor should be located at the beginning of the next (empty) step) Select the “Process Step” item * Other document parts can be inserted the same way: Substrates, Figures, etc. * The Content (TOC) on the last page is an option, but provides a nice overview for very long process flows |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Substrates | | | | | | | | | | |
| Substrate | Orient. | Size | | Doping/type | Polish | thickness | Box | Purpose | # | Sample ID |
| Silicon | <100> | | 100 mm | n (Phos.) | SSP | 525 ±25 µm |  | Device wafers | 2 | S1-S2 |
| Silicon | <100> | | 100 mm | n (Phos.) | SSP | 525 ±25 µm |  | Test wafers | 1 | T1 |

Comments: Number of wafers is for illustration only

|  |  |  |  |
| --- | --- | --- | --- |
| Figures | | | |
| Figure | Caption | Step | Figure |
|  | After SiO2 dep  Not part of this process flow example | 2.1 |  |
|  | After lithography | 3.5 |  |
|  | After BHF etch  Not part of this process flow example | 4.1 |  |
|  | After resist strip  Not part of this process flow example | 4.4 |  |
|  | After lithography  Not part of this process flow example | 5.6 |  |
|  | After metal deposition  Not part of this process flow example | 6.1 |  |
|  | After lift-off  Not part of this process flow example | 6.2 |  |

Comments:Click here to enter text.

|  |  |  |  |
| --- | --- | --- | --- |
| Step Heading | Equipment | Procedure | Comments |
| 1. Preparation | | | **All wafers** |
| * 1. Wafer selection | Wafer box | Take the wafers from the storage and put them in a wafer box. | Note the wafer IDs in the batch traveler |
| 1. SiO2 deposition | | | **All wafers** |
| * 1. Not part of this process flow example |  |  |  |
| 1. Lithography – standard | | | **All wafers** |
| * 1. Surface treatment | BHF dip  *Or*  Oven:  HMDS – 2  *Or*  Spin coater:  Gamma e-beam & UV | BHF dip for Si substrates (BHF: 30 sec, H2O: 5 min)  HMDS treatment for Si, SiO2, and Borofloat  **Recipe:**  01  HMDS priming of silicon substrates  **Recipe:**  0402 DCH 100mm HMDS fast | For Si, choose BHF or HMDS |
| * 1. Clean resist nozzle | Spin Coater: Gamma e-beam & UV | Clean spinner nozzle before every batch  (soak/clean nozzle using acetone, and dispense to get fresh resist) |  |
| * 1. Coat wafers | Spin coater:  Gamma e-beam & UV | **Resist:**  AZ 4562  **Spin:**  30 s @ 2000 rpm (for 10 µm)  **Softbake:**  300 s @ 100 °C proximity 1 mm  **Sequence gamma ebeam & UV:**  4410 DCH 100mm AZ4562 10um | Resist thickness can be measured on FilmTek or ellipsometer  Edge bead removal is possible after coating (separate sequence) |
| * 1. Exposure | Aligner:  MLA1  *Or*  MLA2  *Or*  MLA3 | **Design:**  Your design file  **Exposure dose:**  MLA1: 750 mJ/cm2  MLA2: 750 mJ/cm2 (375 nm)  MLA3: 550 mJ/cm2  **Defocus:**  MLA1: 0  MLA2: 0 (optical AF)  MLA3: 1 | Further information is available on labadviser:  https://labadviser.nanolab.dtu.dk/index.php?title=Specific\_Process\_Knowledge/Lithography |
| * 1. Develop | Developer: TMAH UV-lithography | **Development in TMAH (AZ 726 MIF):**  Multiple puddle, 5 x 60 s  **Sequence:**  (1012) DCH 100mm MP 5x60s |  |
| * 1. Inspection | Optical microscope | Check pattern and alignment marks |  |
| 1. SiO2 etch | | | **All wafers** |
| * 1. Not part of this process flow example |  |  |  |
| 1. Lithography – Lift off | | | **All wafers** |
| * 1. Not part of this process flow example |  |  |  |
| 1. Aluminum pattern | | | **Only device wafers!!** |
| * 1. Not part of this process flow example |  |  |  |
| 1. Linewidth measurement | | | **All wafers** |
| * 1. Not part of this process flow example |  |  |  |

Contents

[1 Preparation 3](#_Toc127864591)

[1.1 Wafer selection 3](#_Toc127864592)

[2 SiO2 deposition 3](#_Toc127864593)

[2.1 Not part of this process flow example 3](#_Toc127864594)

[3 Lithography – standard 3](#_Toc127864595)

[3.1 Surface treatment 3](#_Toc127864596)

[3.2 Clean resist nozzle 3](#_Toc127864597)

[3.3 Coat wafers 3](#_Toc127864598)

[3.4 Exposure 3](#_Toc127864599)

[3.5 Develop 3](#_Toc127864600)

[3.6 Inspection 3](#_Toc127864601)

[4 SiO2 etch 3](#_Toc127864602)

[4.1 Not part of this process flow example 3](#_Toc127864603)

[5 Lithography – Lift off 4](#_Toc127864604)

[5.1 Not part of this process flow example 4](#_Toc127864605)

[6 Aluminum pattern 4](#_Toc127864606)

[6.1 Not part of this process flow example 4](#_Toc127864607)

[7 Linewidth measurement 4](#_Toc127864608)

[7.1 Not part of this process flow example 4](#_Toc127864609)