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Diffusion of $In_{0.53}Ga_{0.47}As$ elements through hafnium oxide during post deposition annealing

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Diffusion of indium through HfO_2 after post deposition annealing in N_2 or forming gas environments is observed in $HfO_2/In_{0.53}Ga_{0.47}As$ stacks by low energy ion scattering and X-ray photo electron spectroscopy and found to be consistent with changes in interface layer thickness observed by transmission electron microscopy. Prior to post processing, arsenic oxide is detected at the surface of atomic layer deposition-grown HfO_2 and is desorbed upon annealing at 350 °C. Reduction of the interfacial layer thickness and potential densification of HfO_2, resulting from indium diffusion upon annealing, is confirmed by an increase in capacitance. © *2014 AIP Publishing LLC*.
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Further scaling for high performance devices has fostered the search of a replacement for Si as the active device channel, with considerable attention on high electron mobility III-V compound semiconductors.[1,2] However, a range of technological challenges need to be resolved before the full potential of III-V channel materials can be realized. There is therefore an active effort to investigate the atomic layer deposition (ALD) and post-deposition processes of high-k dielectrics on III-V substrates to correlate and understand the dependence of electrical properties on the processing conditions.

Wet chemical surface cleaning and pretreatments prior to high-k deposition,[3,4] variation in deposition temperature,[5] and most recently incorporation of III-V barrier layers[6] have all been shown to affect the electrical performance. A "self-cleaning" or "clean-up" phenomenon is believed to lead to reduction of the native oxides initially present on the III-V surfaces during ALD of high-k oxides, particularly using trimethylaluminum (TMA) or tetrakisethylmethylaminohafnium (TEMA-Hf) and water (H_2O).[7–9] Although this process results in an improvement in the electrical properties of high-k/III-V interfaces, the presence of fixed charges and bulk electron/hole traps in the high-k oxide is still an issue for device performance.

As in the silicon technology, post deposition anneals (PDA) in forming gas (FGA) can improve the electrical characteristics of silicon-based devices by reducing the density of interface states (D_{it}).[10] Similarly, electrical measurements have shown that annealing in N_2 and/or FGA can reduce the D_{it} of high-k/III-V gate stacks.[3,11–14] However, the effect of these treatments on the *chemical composition* of the samples has not been fully understood.

It has been suggested, for instance, that PDA could induce changes in interfacial chemical composition due to the thermal instability of the $In_{0.53}Ga_{0.47}As$ native oxides.[15] Decomposed elements from the native oxides could diffuse through the high-k dielectric which would lead to electrical instabilities.[16,17] Most recently, using *ex-situ* hard X-ray photoelectron spectroscopy (XPS), Weiland *et al.*[18] observed Ga and As out-diffusion on $Al_2O_3/In_{0.53}Ga_{0.47}As$ stacks after N_2 annealing at temperatures between 400 °C and 700 °C. In another study, Kang *et al.*[19] noted Ga-O formation on the top surface on $Al_2O_3/HfO_2/GaAs$ gate stacks after PDA at 700 °C. All these studies suggest that III-V substrate elements might diffuse completely through the high-k dielectric film after post deposition anneals, although there have been no unambiguous proof and quantification of such diffusion. It is therefore important to devise experiments with tools that can provide clear evidence for elemental diffusion and changes in the chemical composition of high-k/III-V gate stacks for future production of high mobility devices.

In this work, low energy ion scattering (LEIS), XPS, and transmission electron microscopy (TEM) are used to investigate elemental diffusion, to examine the chemical composition of the surface and near-surface region upon PDA of ALD-grown HfO_2 on $In_{0.53}Ga_{0.47}As$, and to correlate these phenomena to the thickness of the interfacial layer. Furthermore, capacitance-voltage (C-V) and current-voltage (I-V) measurements are performed to determine the effect of the annealing on the maximum accumulation capacitance and oxide leakage in $Pd/HfO_2/In_{0.53}Ga_{0.47}As$ gate stacks.

For this study, $In_{0.53}Ga_{0.47}As$ layers were grown on 50 mm diameter, sulfur-doped InP(100) substrates (doping ~ 3–8 $\times 10^{18}$ cm^{-3}). The buffer layer for $In_{0.53}Ga_{0.47}As$ growth consisted of a 0.1 μm thick sulfur-doped InP (doping ~ 2×10^{18} cm^{-3}). Both the InP buffer and $In_{0.53}Ga_{0.47}As$ top epitaxial layers were grown using metal-organic vapor phase epitaxy. The top epitaxial layer of sulfur-doped $In_{0.53}Ga_{0.47}As$ (doping ~ 4×10^{17} cm^{-3}) was 2 μm thick. The 4 nm-thick HfO_2 films were grown by ALD on the epi-ready $In_{0.53}Ga_{0.47}As/InP$ wafers at 250 °C, using TEMA-Hf and water pulses with an argon carrier gas operating at approximately 0.1 Torr pressure (base pressure < 1×10^{-5} Torr). To maximize the change in the electronic and structural

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properties of the $HfO_2/In_{0.53}Ga_{0.47}As$ MOS system following the forming gas anneal, the as-grown sample was not cleaned (used as is) prior to the deposition of the thin HfO_2 layer by ALD. Consequently, there is interfacial oxide layer between the HfO_2 layer and the $In_{0.53}Ga_{0.47}As$ surface, initially comprised of oxides of indium, gallium, and arsenic.[20] The $HfO_2/In_{0.53}Ga_{0.47}As$ samples were subjected to three different post deposition treatments in this study: (1) no post-deposition anneal, (2) N_2 anneal (at atmospheric pressure) at 350 °C for 30 min, and (3) FGA (5% H_2: 95% N_2 at atmospheric pressure) at 350 °C for 30 min. MOS capacitor structures with a range of gate areas were fabricated by e-beam evaporation of a 200 nm Pd gate using a lift-off process. No ohmic back contact was necessary due to the high doping concentration in the InP substrate and the negligible series resistance.

The choice for the annealing temperature and time included the following factors. First, a wide range of post deposition anneal temperatures from 325 to 700 °C had been reported,[3,11,12,14,18,19] with times varying from 60 s to 1 h. Second, for all studies published to date focusing specifically on diffusion of substrate elements, the lowest temperature reported was 400 °C.[18] The temperature of 350 °C was first selected in this study to assess if diffusion would occur at a temperature lower than employed in previous reports. So an anneal temperature and time were selected to coincide with the anneal conditions reported in studies by Long *et al.*[14] Importantly, samples with post deposition anneal at the same temperature and time in FGA (5% H_2: 95% N_2) and pure N_2 were studied to explore the role (if any) of H_2 in the ambient during the post deposition anneal.

XPS measurements were performed at a scanning angle of 45° with respect to the sample surface using a monochromated Al Kα x-ray source ($h\nu = 1486.7$ eV) and electron detection with a 7 channel hemispherical analyzer operating at a pass energy of 15 eV in an ultra-high vacuum chamber (base pressure of $<5 \times 10^{-10}$ mbar), as described in more detail elsewhere.[21] Spectral peak deconvolution was carried out using the Analyzer peak fitting software, which allows for independent control of the Gaussian and Lorentzian peak components, as well as for dynamically fitting the peak background during the fitting process. This procedure provides a much more accurate background subtraction.

LEIS was used to examine the surface composition with high depth resolution for elements such as metal and oxygen.[22] Analysis was performed in a chamber equipped with an IonTOF Qtac[100] detector using 3-keV $^4He^+$ and 5-keV Ne+ under UHV conditions (base pressure $< 7 \times 10^{-10}$ mbar). Typical measurements used a target ion current in the range of 3 nA. The ion beam was focused on a 1 mm × 1 mm sample area at normal incidence. The high surface sensitivity of the technique (~3 monolayers) originates from a unique analyzer detector design, where the large scatter angle (fixed scattering angle = 145°) of detection increases elemental sensitivity, allowing low ion doses (negligible sputtering/intermixing). Initially, the He^+ LEIS spectra, using a $\sim 9 \times 10^{13}$ ion/cm^2 dose, were typically dominated by carbon contamination from air-exposure during sample transfer from the ALD reactor to the LEIS instrument, due to the high surface sensitivity of the technique. To address this issue, the samples were lightly sputtered[23] for 120 s using 10^{15} Ne^+ ions/cm^2 (5 keV). Sputtering was stopped immediately after the carbon levels, monitored using He^+ ions, were below the LEIS detection limit for carbon (C > 1% of monolayer [10^{15}/cm^2]).[22,23] To better distinguish heavier elements such as Ga, As, and In, Ne^+ ions ($\sim 7 \times 10^{13}$/cm^2) were used.

Conventional TEM samples were prepared using ion beams in a Helios 600 workstation and examined with a JEOL2100 at 200 kV.

Figure 1 shows the XPS core level spectra of (a) Ga $2p_{3/2}$, (b) As $2p_{3/2}$, and (c) In $3d_{5/2}$ for all three $HfO_2/In_{0.53}Ga_{0.47}As$ samples, untreated, and treated in N_2 and FGA at 350 °C, respectively. The thickness of the HfO_2 film (4 nm) ensures that the substrate is not detected, as evidenced by the absence of bulk contribution from the any of the core level spectra (Figures 1(a)–1(c)). Considering the relative core level kinetic energy for Ga $2p$ (binding energy = 1117 eV), the photoelectron kinetic energy is 370 eV and the effective attenuation length (EAL) 0.6 nm, such that the total XPS sampling depth is ~2 nm.[24,25] This indicates that no Ga contribution from the bulk $In_{0.53}Ga_{0.47}As$ could be observed within the XPS detection limits, so that only Ga located near the top surface region would appear in the spectra. This initial observation establishes a baseline necessary to draw conclusions, if any, of the substrate elements that are detected within or at the surface of the

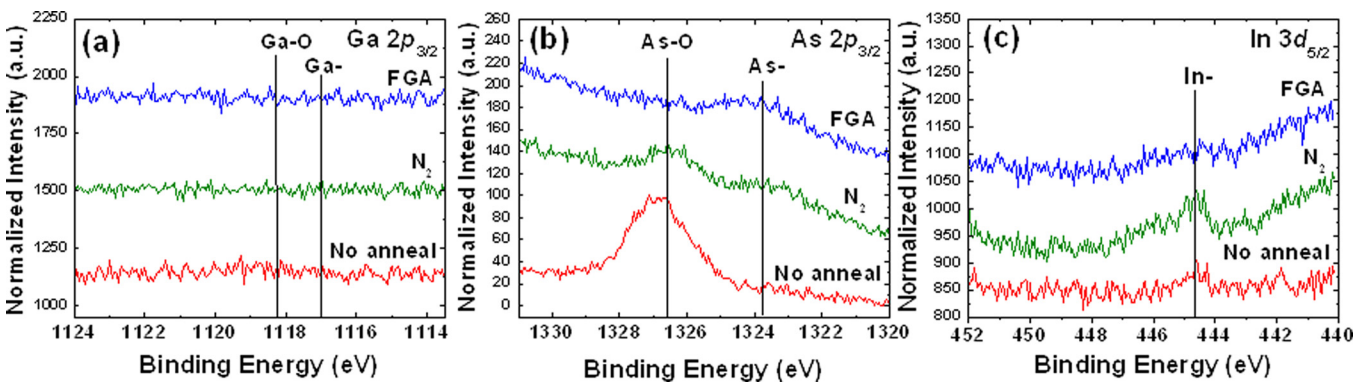

FIG. 1. XPS core level spectra of (a) Ga $2p_{3/2}$, (b) As $2p_{3/2}$, (c) In $3d_{5/2}$ for $HfO_2/In_{0.53}Ga_{0.47}As$ after post deposition treatment in N_2 (green), FGA (blue), and unannealed samples (red).

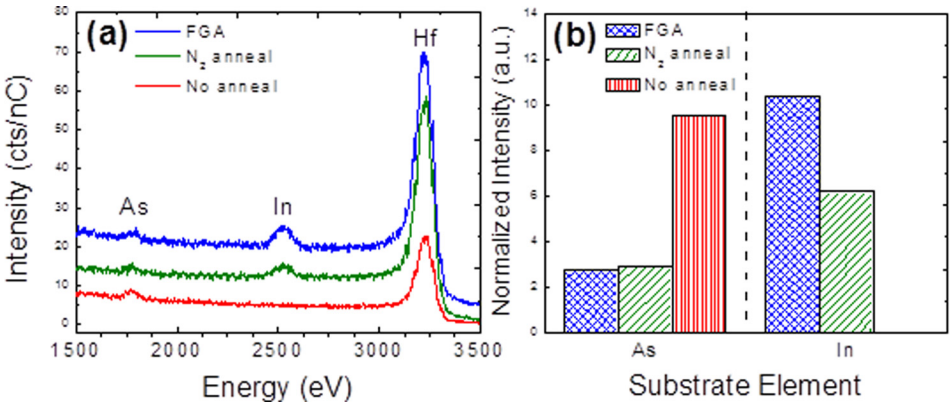

FIG. 2. (a) LEIS spectra and (b) normalized LEIS peak intensities of 5 keV Ne^+ backscattered from $HfO_2/In_{0.53}Ga_{0.47}As$ after post deposition treatment using FGA, N_2 anneal and no anneal samples of the diffused substrate elements through. Evidence of As and In indicates element at the top most monolayer. No In is detected on the "no annealed" sample. The surface was lightly sputtered prior to analysis.

HfO_2 layer. The fact that an As signal is observed (As 2*p*) for all three samples after HfO_2 deposition, including on the sample prior to any annealing (Figure 1(a)), indicates that As migrates to the surface *during* the ALD process since electrons from the As 2p level have a slightly smaller effective attenuation length (EAL = 0.45 nm) than electrons from the Ga 2*p* core level. Since these samples were exposed to atmosphere prior to XPS, any As present at the surface would be expected to oxidize as is seen on the unannealed sample. Upon a post deposition anneal at 350 °C, the As oxide signal is reduced with a corresponding increase of the reduced As. Hydrogen contained in forming gas is clearly more effective to reduce As oxide than N_2. Overall, there is no evidence that As located at the surface after ALD is removed upon annealing.

In contrast, a slight In $3d_{5/2}$ signal (close to the XPS detection level) is detected after HfO_2 deposition prior to any annealing. This observation suggests that In has partially diffused into the film during the ALD process. Upon annealing at 350 °C in N_2, the In peak intensifies, suggesting that In continues to outdiffuse from the interfacial layer or the $In_{0.53}Ga_{0.47}As$ surface through the high-k dielectric. This is also expected for the FGA-treatment at 350 °C but the lower In core level intensity suggests that it may desorb from the surface, since In and As oxides are known to begin to decompose at temperatures as low as 150 °C.[15] The relative position of the diffused elements is best investigated by LEIS, which can only sensitively examine the first few monolayers (<3 monolayers) of the HfO_2/InGaAs surface, using 5 keV Ne^+ ions. Figure 2 shows (a) LEIS spectra and (b) peak intensities of the ions backscattered from the HfO_2 surface after deposition, N_2 annealing and FGA treatments for In and As. All peak intensities are normalized to the Hf peak in order to compare the relative As and In coverages. An intense As signal is observed at the surface after ALD of HfO_2. This unambiguously shows that part of the As $2p_{3/2}$ core level electrons observed with XPS in Figure 1(a) originates from the surface. In contrast, no In signal is observed for this unannealed sample, highlighting the difference in mobility between As and In atoms during ALD growth. While In does diffuse into HfO_2, as evidenced by a very weak In $3d_{5/2}$ core level signal in XPS, it does not reach the near surface region. After the N_2 anneal, the normalized As signal intensity is reduced compared to the unannealed sample, suggesting that surface As does desorb from the surface at these temperatures, as postulated above. The appearance of an In signal in the LEIS spectra after annealing is evidence for In diffusion from the HfO_2 interfacial region to the surface. Since the XPS measurements of In $3d_{5/2}$ indicate an overall decrease of In, this observation indicates that In has diffused to the surface and part of it desorbed. While this suggests that hydrogen fosters desorption, the role of hydrogen is still not well understood.

In order to understand the effects of post-deposition annealing on the interfacial structure of the $Pd/HfO_2/In_{0.53}Ga_{0.47}As$, conventional TEM images were obtained on all three samples after treatment (Figures 3(a)–3(c)). For the untreated sample, a clear interfacial region is observed between the HfO_2 and $In_{0.53}Ga_{0.47}As$. This interfacial layer is most likely composed of native oxides.[20] Importantly, a reduction in the interfacial layer thickness is observed after annealing the $HfO_2/In_{0.53}Ga_{0.47}As$ stack in N_2 at 350 °C. Further reduction of this interfacial layer is observed when the

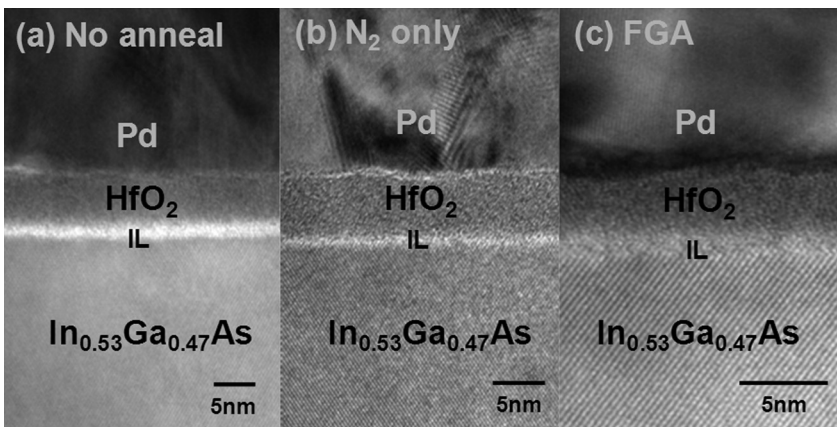

FIG. 3. Conventional TEM images of (a) no anneal, (b) N_2 only, and (c) FGA $Pd/HfO_2/In_{0.53}Ga_{0.47}As$ gate stacks showing the interfacial layer reduction after the post oxide deposition anneal.

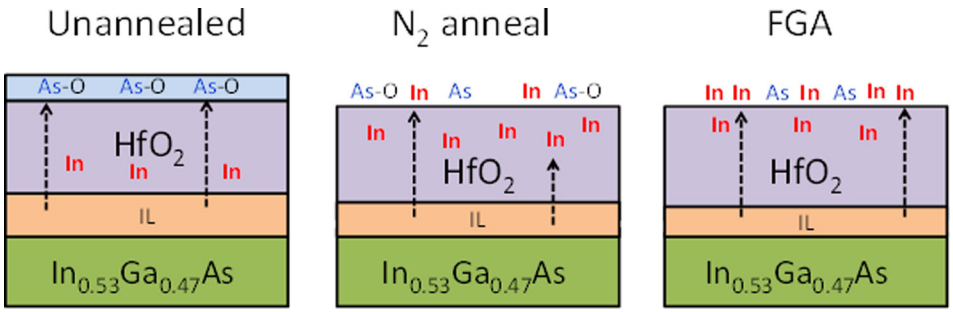

FIG. 4. Schematic representation of the substrate element diffusion through the HfO_2. The net result of these processes is a reduction of interfacial layer thickness, and potentially a densification of the HfO_2 layer, arising from the ability of excess oxygen to reduce the number of oxygen vacancies in layer HfO_2 layer. A natural consequence of these phenomena should lead to measurable changes in electrical properties of the stack.

sample undergoes the FGA treatment. These observations are consistent with the loss of elements (by diffusion) observed with XPS and LEIS as well as IR measurements.[26] They support the conclusion that In observed at the surface and near surface region is due to the diffusion from the decomposition of the interfacial layer during post deposition treatments.

Figure 4 schematically illustrates the proposed mechanisms derived from the combined XPS, LEIS, and TEM measurements. First, the unannealed samples display a large concentration of As at the surface of HfO_2 in the form of As oxides, with a corresponding modification of the interfacial layer. This interfacial layer contains less As oxide than the native oxide due to oxygen scavenging during the initial ALD process.[7,9,27] Such As depletion is expected to result in a relatively In- and Ga-rich interfacial layer. During N_2 anneal, surface As species are desorbed, most likely in the form of As-O. Concurrently, In originating from the In- and Ga-rich interfacial layer, migrates through the HfO_2 layer to the surface and near surface region.

As previously suggested only from XPS measurements, thermal treatments lead to interfacial layer decomposition and diffusion.[15,17,28] For instance, Suri *et al.*[28] established from *ex-situ* XPS that after depositing an HfO_2 film on native oxide-covered GaAs, no arsenic oxides are observed after a 400 °C rapid thermal anneal for 20 s in a N_2 environment. Their observation is consistent with the well-established chemical reduction of As_2O_3 on GaAs surfaces between the temperatures of 320 °C–400 °C, following the reaction:[29,30]

$$As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 2As_2(\uparrow)$$

This chemical pathway provides the formation of a strongly bound Ga_2O_3 moiety at the interface, which is a stable oxide in this temperature range. This accounts for a lack of Ga signal in both XPS and LEIS data. Chang *et al.*[31] also observed an increase of the In $3d_{3/2}$ core level using angle-resolved XPS after depositing ultra-thin (0.8 nm) HfO_2 films by ALD on $In_{0.2}Ga_{0.8}As$ at 320 °C, which they attributed to In segregation.

In our case, we find that the mobility of the substrate atoms strongly depend on the deposition temperature. At 250 °C deposition temperature, no indium is observed by LEIS at the HfO_2 surface. Upon annealing in nitrogen or forming gas at 350 °C, In diffuses to the HfO_2 surface, in agreement with the observations of Chang *et al.*[31] A further increase in the In concentration after FGA treatment suggests that H_2 also plays a role in the decomposition of the interfacial oxides. Such decomposition gives rise to excess oxygen at the interface, which may naturally migrate to vacancy sites within the HfO_2 layer[32] and would result in modification (e.g., densification) of the HfO_2 layer itself. The In component, believed to be in the form of In-O_x, is located within the top most monolayers of the HfO_2 surface since it is easily detected by a highly surface sensitive technique (LEIS). In addition, the relatively more intense indium peak in LEIS after FGA as compared to N_2 anneal is consistent with an accumulation of In at the surface. All these results are consistent with the current observation for HfO_2 films on $In_{0.53}Ga_{0.47}As$, suggesting that diffusion is a general phenomenon for high-*k* dielectric/III-V stacks that are typically characterized by unstable interfaces.

From all these observations, we hypothesize that post annealing, particularly in forming gas, reduces the interfacial layer and potentially decreases the number of oxygen vacancies in the HfO_2 films by oxygen migration from the interface upon In diffusion. To test this hypothesis, C-V measurements were performed using the as-deposited (unannealed) stack as reference. These C-V measurements recorded over a range of frequency and temperature were sufficient to show that the as-deposited $HfO_2/In_{0.53}Ga_{0.47}As$ stack and subsequently annealed (in N_2 or FGA) samples all exhibit genuine surface accumulation, and that the accumulation capacitance is affected by the annealing process.

The results in Table I illustrate that the post-deposition treatments of HfO_2/InGaAs gate stacks result in an increase in the maximum capacitance upon N_2 anneal and even larger increase upon FGA in the accumulation region at 3 V. The accumulation capacitances in the C-V response for the no anneal, N_2 and FGA samples have the capacitance equivalent thickness (CET) values of 1.92 nm, 1.82 nm, and 1.63 nm, respectively. It is noted that these experiments used intentionally non-optimized stacks in order to highlight interface layer modification and elemental diffusion resulting from post deposition annealing. The interface state density around the mid gap energy D_{it} was in excess of $1 \times 10^{13}\,cm^{-2}\,eV^{-1}$ for all samples. Importantly, the leakage was $<5 \times 10^{-4}$ A/cm^2 over the C-V bias range (±3 V), allowing reliable capacitance extraction for the values reported in Table I. Overall, these results are fully consistent with the observed reduction of interfacial oxide by TEM (see supplementary material[26]).

TABLE I. Maximum capacitances (C_{max}) and CET for post deposition-treated $HfO_2/In_{0.53}Ga_{0.47}As$ samples.

Sample	No anneal	N_2 only	Forming gas
C_{max} @ 1 kHz(μF/cm^2)	1.85	1.90	2.11
CET @ = +3 V (nm)	1.92	1.82	1.63

In summary, $HfO_2/In_{0.53}Ga_{0.47}As$ gate stacks were characterized using LEIS, XPS, and C-V measurements. Transport of As, and to a much lower degree of In, both originating from the initial native oxide, was shown to occur *during* ALD of HfO_2, as evidenced by the detection of As-based oxides in XPS and surface As with LEIS on unannealed samples. No In or Ga was detected on the HfO_2 *surface* prior to any post-annealing treatments, highlighting the mobility of As compared to these two elements. Clear evidence for In diffusion to the surface *only* after post-deposition annealing of $HfO_2/In_{0.53}Ga_{0.47}As$ stacks was provided by XPS and LEIS. TEM images showed that the thickness of the interfacial layer is decreased upon annealing, confirming out-diffusion of metallic elements and suggesting oxygen depletion as well. The overall reduction of the interfacial layer and postulated densification of the HfO_2 layer upon post deposition anneals in N_2 anneal or forming gas is further supported by the observed increase in the maximum capacitance.

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