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Cite as: J. Vac. Sci. Technol. A **38**, 053002 (2020); <https://doi.org/10.1116/6.0000357>

Submitted: 27 May 2020 . Accepted: 01 July 2020 . Published Online: 24 July 2020

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# Ultrahigh aspect ratio etching of silicon in SF<sub>6</sub>-O<sub>2</sub> plasma: The clear-oxidize-remove-etch (CORE) sequence and chromium mask

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Submitted: 27 May 2020 · Accepted: 1 July 2020 ·

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## ABSTRACT

Getting high aspect ratio (HAR) structures is a frequent request in directional etching of silicon using mainstream plasma tools. HAR features are useful either directly (e.g., photonic devices) or as a template for constructing more complicated structures (e.g., metamaterials). The latter is possible by adding postetch procedures such as atomic layer deposition. In this study, a procedure to fabricate ultra-HAR nanostructures is demonstrated. It is built on a recently developed highly directional plasma etch procedure operating at room temperature called CORE (meaning clear, oxidize, remove, and etch) in which the usual fluorocarbon (FC) inhibitor of the Bosch process is replaced by oxygen. The effect of different CORE parameters on the etch rate and profile is investigated and optimized with respect to low mask undercut and high directionality. Due to the self-limiting property of the oxidation step, the CORE sequence is different from FC-based sequences, particularly concerning what type of etch mask is preferable. We show that 60 nm of chromium masking is well suited for ultra-HAR etching without complicating the plasma process or compromising the overall fabrication procedure. The nanopillar arrays (200 nm diameter, 400 nm pitch and 60 nm diameter, 500 nm pitch) have smooth straight sidewalls with aspect ratios beyond 55 for gaps and up to 200 for pillars. Due to the very mild plasma condition (less than 40 W RIE power), the mask selectivity with respect to silicon can be tuned above 500. In addition, the clean operation of the CORE sequence (no FC pileup as is typical in the Bosch process) prevents time-consuming profile tuning and enables process freedom and reproducibility.

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## I. INTRODUCTION

The importance of anisotropic etching dates back to the introduction of semiconductor fabrication in the early 1970s to increase device density. In particular, the need for high aspect ratio (HAR) etching (say AR > 10) has been of interest for the semiconductor industry to enable trench DRAM capacitors, trench MOSFET isolation, or FinFETs. Aspect ratio is defined as the depth of a trench/hole or height of a plate/pillar divided by its width/diameter. In addition to large scale integrated circuit manufacturing, HAR structures are increasingly requested in applications such as biological or chemical sensors,<sup>1–4</sup> electronic devices,<sup>5–7</sup> energy conversion and solar cells,<sup>8,9</sup> photon-absorbent surfaces,<sup>10</sup> confined phonon or photonic devices,<sup>11,12</sup> and quantum-based devices.<sup>13</sup> The success of

HAR etching depends on controlling the lateral etch rate while keeping or enhancing the vertical etch rate. In general, wet chemical etching is not suitable for HAR fabrication due to sloped walls and/or severe mask undercutting (with the notable exceptions of metal assisted chemical etching or <110> single crystalline silicon etching).<sup>14–18</sup> Instead, dry plasma etching has proven to faithfully transfer the requested mask pattern into the underlying silicon.<sup>19–28</sup> The maximum ratio between the vertical and horizontal etch is mostly depending on the directionality of the incoming ions, so the ion angular distribution function (IADF) is an important plasma parameter to consider in HAR etching. Modern HAR processes tend to minimize the reactor pressure and increase the self-bias during the etch process as this sharpens the IADF even though this compromises mask selectivity.

In this work, a simple, reliable, and reproducible procedure is developed to fabricate ultra-HAR nanofeatures using the CORE (meaning clear, oxidize, remove, and etch) sequence and the chromium mask. The CORE sequence is a recently developed highly directional plasma etch procedure in which the fluorocarbon (FC) inhibitor of the Bosch process is replaced by oxygen.<sup>29–31</sup> It is related to the conventional mixed mode plasma etching in which SF<sub>6</sub> and O<sub>2</sub> are inserted simultaneously,<sup>32–34</sup> but this time, the gases enter the reactor sequentially. The effect of different CORE parameters (e.g., O-time, R-power, and E-pressure) on the etch rate and the profile are carefully investigated and optimized with respect to low mask undercut, smooth sidewall, high directionality, and ultra-HAR ability. Since CORE uses a switching sequence of SF<sub>6</sub> and O<sub>2</sub> plasma, it has limited selectivity toward the usual photoresist mask. Therefore, in order to have sufficient selectivity that enables ultra-HAR etching, chromium is utilized as a mask. However, it is known that chromium is damaged (or etched) when exposed to plasma ash systems and O<sub>2</sub> is a basic ingredient of the CORE sequence.<sup>35–38</sup> Therefore, a further task of this study is to find the limits of ultra-HAR etching using chromium as a hard mask.

## II. MATERIALS AND METHODS

The procedure to sculpture ultra-HAR structures uses the following cleanroom processes. First, resist patterns are created using DUV stepper lithography (200 nm dots, 400 nm periodicity) or electron beam (e-beam) lithography (60 nm dots, 500 nm periodicity). Subsequently, the stepper BARC layer or e-beam residue is removed with plasma oxygen. Then, chromium is deposited and lift-off is performed. Chromium is easily integrated in standard semiconductor process flows because it can be stripped conveniently using plasma ashing tools. Finally, silicon is etched using the CORE sequence, and the samples are characterized using scanning electron microscopy (SEM, Supra V60, Zeiss) that allows for a 10 nm resolution. The details of the process flow are described below.

### A. Stepper

Silicon wafers (150 mm diameter Czochralski, 675 μm thick, 5–10 Ω cm phosphorous-doped n-type, <100> orientation) are coated with 65 nm BARC (DUV42S-6) and 360 nm DUV resist (KRF 230Y) using a spin coating system (Gamma 2M spin-coater, Süss MicroTech). Then, pillar patterns are defined by a DUV stepper (FPA-3000EX4, Canon) equipped with a 248 nm KrF excimer laser. The exposure dose is 86 mJ/cm<sup>2</sup>. Then, the wafers are developed in 2.38% tetra-methyl-ammonium-hydroxide in water (AZ726 MIF, AZ Electronic Materials), rinsed in de-ionized (DI) water, and spin dried with a gentle nitrogen stream. Finally, the BARC layer is etched using an RIE system providing oxygen plasma.

### B. E-beam

For nanosized patterns between 30 and 100 nm, a 100 kV e-beam writing system (JEOL JBX-9500FSZ) scanning with 10 nm steps is used. A positive tone e-beam resist ZEP520A (ZEON)

having a thickness of 145 nm is spin-coated for 60 s at 4000 rpm followed by baking for 3 min at 180 °C. During exposure, the electron current is set at 12 nA with 10 nm spot size and dose between 293 μC/cm<sup>2</sup> (30 nm lines) and 263 μC/cm<sup>2</sup> (100 nm lines). Exposed samples are developed for 180 s with ZED-N50 (*n*-amyl acetate) and rinsed with isopropanol alcohol (IPA). Then, the wafers receive a short descum to remove any surface resist residue. For this, a barrel etcher including a Faraday cage (Tepla 300 Semi-Auto) is used for 10 min at room temperature with 500 SCCM O<sub>2</sub> at 1 mbar and 150 W.

### C. Chromium deposition and lift-off

After photoresist patterning and BARC removal, the deposition of 30 or 60 nm chromium is performed using a conventional e-beam evaporator (Temescal FC-2000, Ferrotec). The deposition rate is kept at 5 Å/s and the base pressure at 10<sup>-6</sup> Torr. The lift-off is done by placing the wafers into an ultrasonic bath containing *N*-methyl-2-*N*-pyrrolidone (Remover 1165) for a few minutes, followed by a 5 min rinse in IPA. The lift-off from DUV stepper patterned wafers becomes a more complicated procedure since Remover 1165 cannot dissolve photoresist properly, probably due to chromium deposition on the sidewall of the positive tone DUV polymer. The problem is solved by placing the wafer into a beaker containing 250 ml DI water and adding 500 ml sulfuric acid (H<sub>2</sub>SO<sub>4</sub>). The solution develops heat and the lift-off eventually succeeds leaving only a hard mask pattern attached to the silicon substrate. After 10 min, the wafer is taken out and properly rinsed in DI water. Finally, to verify the critical dimension of the retrieved patterns, the samples are inspected using an optical microscope (Nikon Eclipse L200) that allows a measurement resolution of 200 nm.

### D. Silicon etching

After lift-off, the samples are cleaved manually into pieces of around 1 × 1 cm<sup>2</sup> and attached on a 150 mm silicon carrier wafer by a small drop of Galden PFPE fluid (Solvay Solexis SpA). The PFPE fluid is a chemically inert perfluoropolyether vacuum oil with good thermal conductivity. Finally, the etch process is performed in a dual source plasma system (DRIE Pegasus, SPTS) operating in the RIE mode (i.e., no ICP power). The schematic illustration of the SPTS Pegasus system is shown in Fig. 1. The system has been dedicated for SF<sub>6</sub>/O<sub>2</sub> based plasma etching solely and has no prior FC history. This FC-free chamber is needed to ensure the absence of any contamination or influence on the fragile oxygen plasma oxidation that is required for the CORE sequence.

## III. RESULTS AND DISCUSSIONS

The procedure to create ultra-HAR nanostructures is based on the recently developed four steps CORE sequence operating at room temperature as schematically shown in Fig. 2. It uses a sequence of sulfur-hexafluoride (SF<sub>6</sub>) plasma to etch silicon (the E-step), repeatedly alternated with oxygen (O<sub>2</sub>) plasma to passivate the etched features (the O-step). Both steps operate at a relatively high pressure above 20 mTorr to ensure low mask erosion. The extra R-step uses ion energy at a very low pressure (0.2 mTorr) to

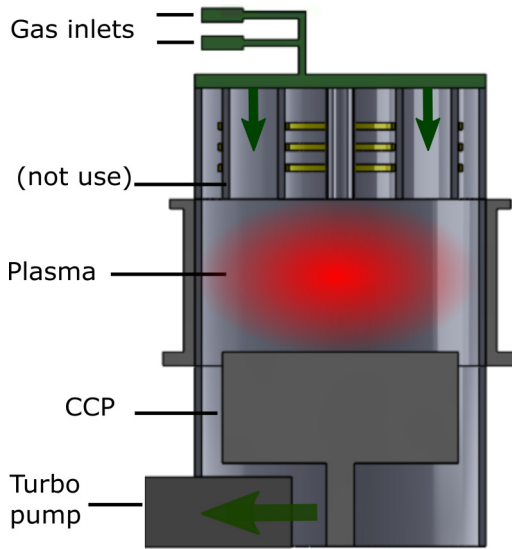


FIG. 1. Schematic illustration of the SPTS Pegasus etch system.

ensure high directionality. It is included after the O-step to remove the passivation layer on horizontal surfaces but leaving the vertical wall passivation intact. The C-step is added to flush the reactor from remaining  $\text{SF}_6$  gas and  $\text{SiF}_4$  reaction products. Finally, the plasma is solely generated by the RIE (i.e., platen) source as the ICP source without a protective Faraday cage has a substantial risk of generating  $\text{AlF}_x$  particles.

In Secs. III A–III G, the effect of different CORE parameters on the etch rate and the profile is investigated using the initial CORE recipe shown in Table I, including a guideline to tune nano-scale pillar arrays for ultra-HAR.

### A. Effect of O-parameters

In the CORE sequence, oxygen is used instead of FC to protect the silicon sidewall during etching. Therefore, the effect of oxidation (O-) power  $P_O$  and time  $t_O$  on the etch profile is investigated. First, the O-power is increased from 10 to 20 W while keeping other parameters in Table I fixed. When the O-power is at 10 W [Fig. 3(a)], the etch profile is deeper with stronger undercut at the top part compared to 15 W [Fig. 3(b)] and 20 W [Fig. 3(c)]. Meanwhile, the chromium mask is eroded independent of the O-power at a rate of  $\sim 2$  nm/h. This is because the produced bias and plasma potential during the O-step is too low to have a noticeable effect on the mask erosion rate. There is a strong undercut at 10 W as the oxygen plasma is believed to be too weak to completely protect the sidewall from the attack of fluorine radicals during a comparatively long E-time in the CORE cycle. Above 15 W, the profile and undercut have no noticeable improvement. This might be because at 15 W the oxygen plasma is already fully dissociated. Therefore, in order to further increase the sidewall protection and reduce the mask undercut, the oxidation time  $t_O$  is increased from 4 to 8 s [Fig. 3(d)]. However, the consequence of longer oxidation time is that the profile becomes positive, which restricts the fabrication of ultra-HAR structures.

### B. Effect of R-parameters

In order to make the etch profile in Fig. 3(d) straight, the removal power ( $P_R$ ) and time ( $t_R$ ) are varied. As shown in Fig. 4, when  $P_R$  is increased from 18 W [Fig. 4(a)] to 22 W [Fig. 4(b)], the profile straightens. The produced DC bias at 18 and 22 W is 32 and 48 V, respectively. When the DC bias increases, it will sharpen the ion angular distribution. Thus, most ions will bombard the bottom of the features resulting in a straight profile. Furthermore, the erosion rate is 2 nm/h at 18 W and  $2\frac{1}{2}$  nm/h at 22 W, so it scales almost linearly with R-power. Consequently, the selectivity toward silicon decreases from 450 ( $P_R=18$  W) to 370 ( $P_R=22$  W).

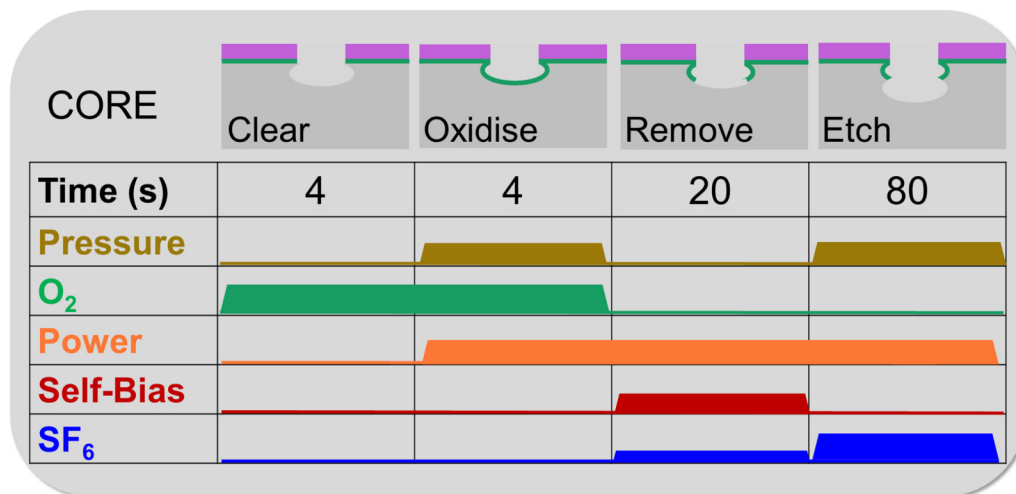


FIG. 2. Schematic illustration of the CORE sequence.

**TABLE I.** Initial CORE recipe to study ultra-HAR silicon nanoscale etching.

CORE	C	O	R	E
Time (s)	4	4	20	80
Pressure (mT)	0.8	50	0.2	24
O <sub>2</sub> (SCCM)	50	50	0	0
Platen power (W)	0	10	18	15
DC self-bias (V)	0	0	32	0
SF <sub>6</sub> (SCCM)	0	0	5	10

To improve the selectivity, one might opt for a shorter R-time as shown in Fig. 4(c), where  $t_R$  is decreased from 20 to 16 s. Indeed, the selectivity improves to 400, but the profile becomes positive again. So both higher power and longer removal time will straighten the profile but will also erode the chromium mask faster. Therefore, it is important to limit  $P_R$  and  $t_R$  to be just enough to straighten the profile in order to preserve the mask as much as possible.

### C. Effect of E-parameters

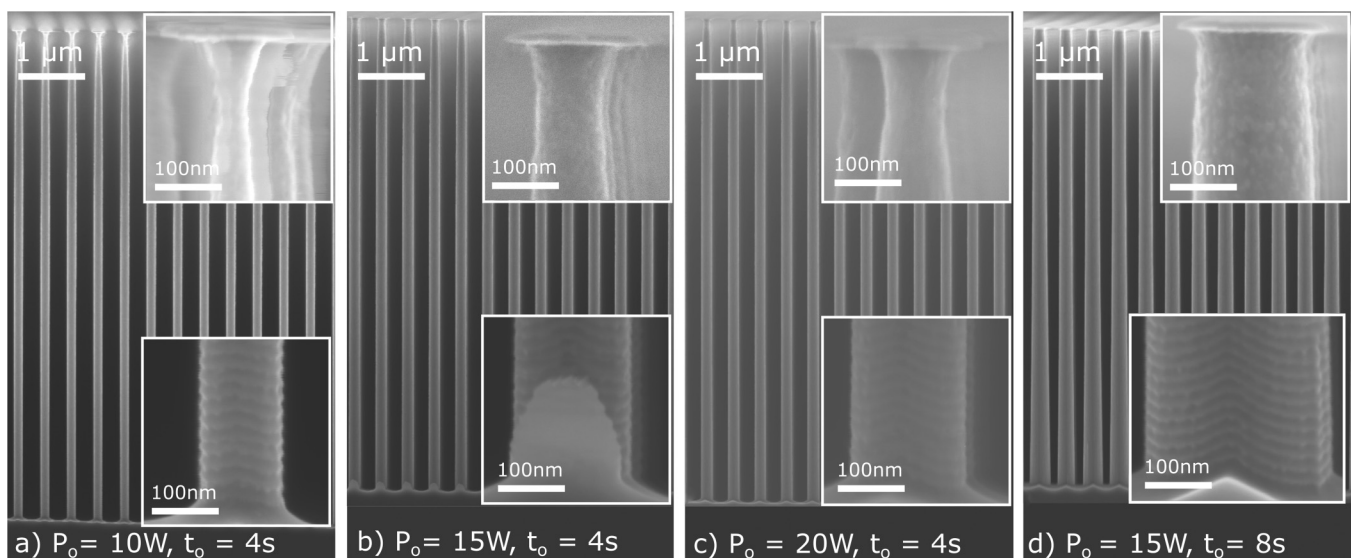
A basic part of the CORE sequence is the etching (E-) step. In this step, SF<sub>6</sub> gas is inserted into the reactor and transformed into plasma with the aid of a 13.56 MHz radio frequency platen source. Before the effect of the E-parameters is discussed, a few plasma concepts will be highlighted in order to understand the observed behavior.

Prominent constituents of the plasma are electrons, ions, radicals, and photons. The electrons are accelerated by the platen power and consequently gain large amounts of kinetic energy (expressed by the electron temperature  $T_e$ ) but sooner or later will inelastically collide with SF<sub>6</sub> molecules and produce many species

by dissociation, ionization, attachment, and excitation.<sup>39,40</sup> When an electron collides “soon” with an SF<sub>6</sub> molecule, it can only excite the molecule that gives the plasma its characteristic glow. If the electron is able to escape an early collision, its kinetic energy might be high enough to dissociate an SF<sub>6</sub> molecule and create F radicals. The latter F radical is responsible for etching following the reaction  $\text{Si} + 4\text{F} \rightarrow \text{SiF}_4$ . If the electron collides “later” and gains energy beyond several electron volts, the collision will cause ionization such as  $e^- + \text{SF}_6 \rightarrow 2e^- + \text{SF}_5^+ + \text{F}$ . The extra electron is needed to sustain the plasma as it will trigger a cascade reaction of additional electrons. Even though the electron temperature  $T_e$  (eV) is the main drive underneath the etch process, the common parameters to vary are the (platen) power  $P_E$  (W), SF<sub>6</sub> flow  $Q_E$  (SCCM), and the process pressure  $p_E$  (mTorr). Therefore, it is important to predict how these parameters affect  $T_e$ . In a previous study, it has been found for a fairly identical plasma system that the etch rate has a maximum when the following relation between P, Q, and p is met: (1) the flow is set at 0.2 SCCM per W and (2) the pressure is set at 0.15 mTorr per SCCM.<sup>41</sup> So, if a power of 15 W is selected, then the highest etch rate is found at 3 SCCM and 0.45 mT. When the flow is lower, for example, 2 SCCM, there is not enough SF<sub>6</sub> available to produce the highest possible active fluorine concentration out of the supplied power. This is called the flow-limited regime where additional power has a minor effect on the etch rate. In contrast, when the flow is increased to 6 SCCM, not sufficient energy is available to break all the bonds and much incoming SF<sub>6</sub> gas is unused. This is the power-limited regime where additional flow has almost no influence on the etch rate.

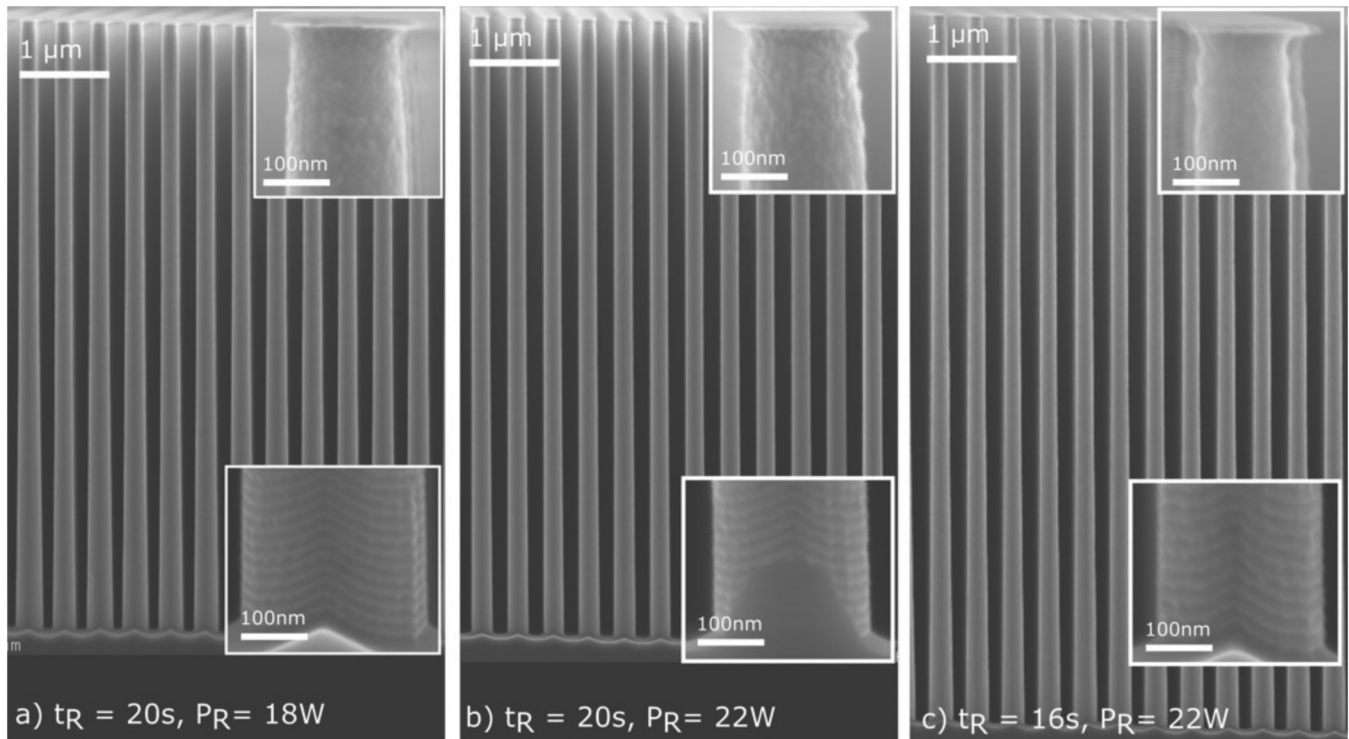
#### 1. E-power

First, the SF<sub>6</sub> flow rate is fixed at 15 SCCM, and the valve position is fixed at 2%. This corresponds to a process pressure of



**FIG. 3.** Effect of changing the O-power [(a)–(c)] and time (d) on the etch profile.





**FIG. 4.** Effect of changing the R-power [(a) and (b)] and time (c) on the etch profile.

36 mTorr. Then, the plasma power  $P_E$  is increased from 10 to 20 W as shown in Fig. 5. The power increase is in the range of the power-limited regime. Therefore, as expected, the pillar height increases almost linearly with increasing plasma power, i.e.,  $5.0\ \mu\text{m}$  at 10 W,  $6.6\ \mu\text{m}$  at 15 W, and  $8.8\ \mu\text{m}$  at 20 W. Since the R-step is fixed, the mask erosion rate is not affected. Therefore, the Cr/Si selectivity will increase linearly with increasing power. However, there is a difference in the etch profile when the plasma power increases. At 10 W, the etch profile is positive [Fig. 5(a)], while at 15 W, it becomes straighter [Fig. 5(b)] and even more so at 20 W [Fig. 5(c)]. Furthermore, the higher the plasma power the stronger the lateral etch and mask undercut. This is a direct consequence of the increased fluorine pressure that erodes the fragile oxide sidewall and makes the pillars thinner. As a result, the ultrathin pillars ( $AR \approx 200$ ) tend to collapse and stick together while performing SEM imaging as observed in Fig. 5(c). This collapse during SEM imaging can be prevented by scanning the electron beam along the pillar direction instead of perpendicular. It is an interesting topic and deserves more attention, but “electronic pillar actuation” is besides the focus of this study.

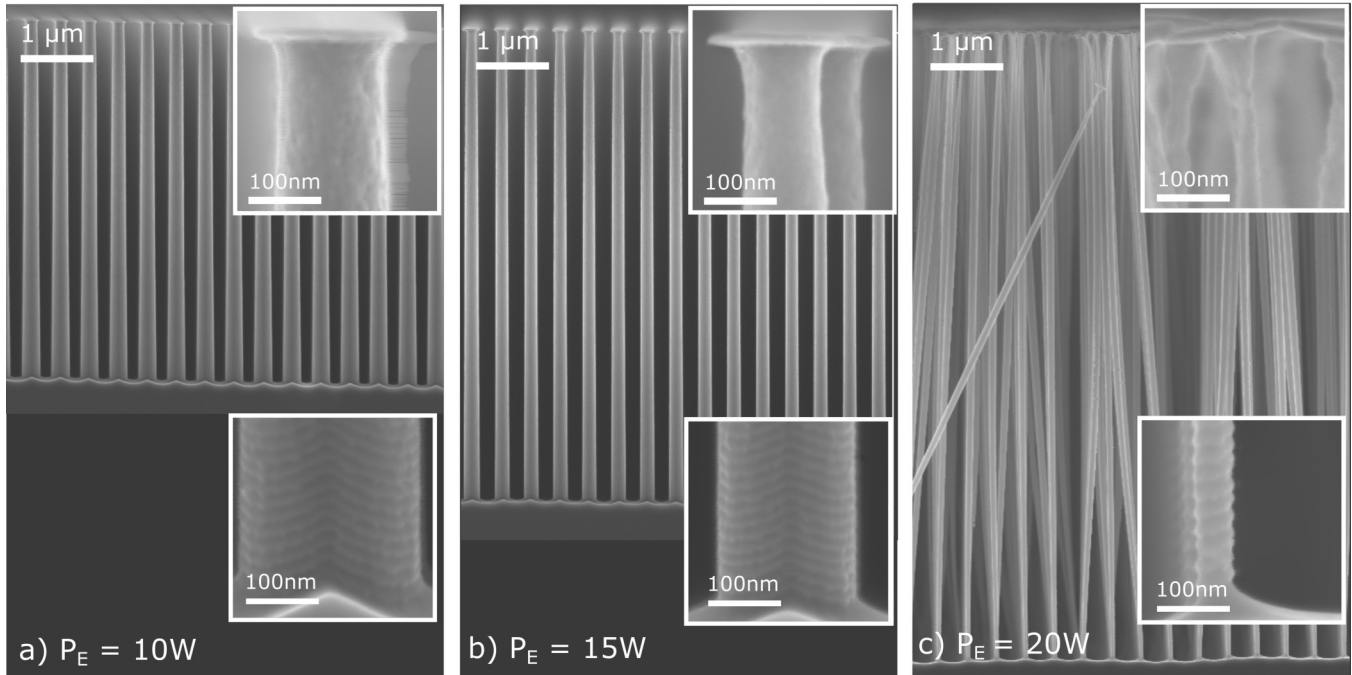
## 2. E-pressure

Next, both the  $\text{SF}_6$  flow (10 SCCM) and the plasma power (15 W) are fixed and the pressure  $p_E$  is increased by closing the valve between 2% (24 mT) and 1% (54 mT). It is observed in Fig. 6

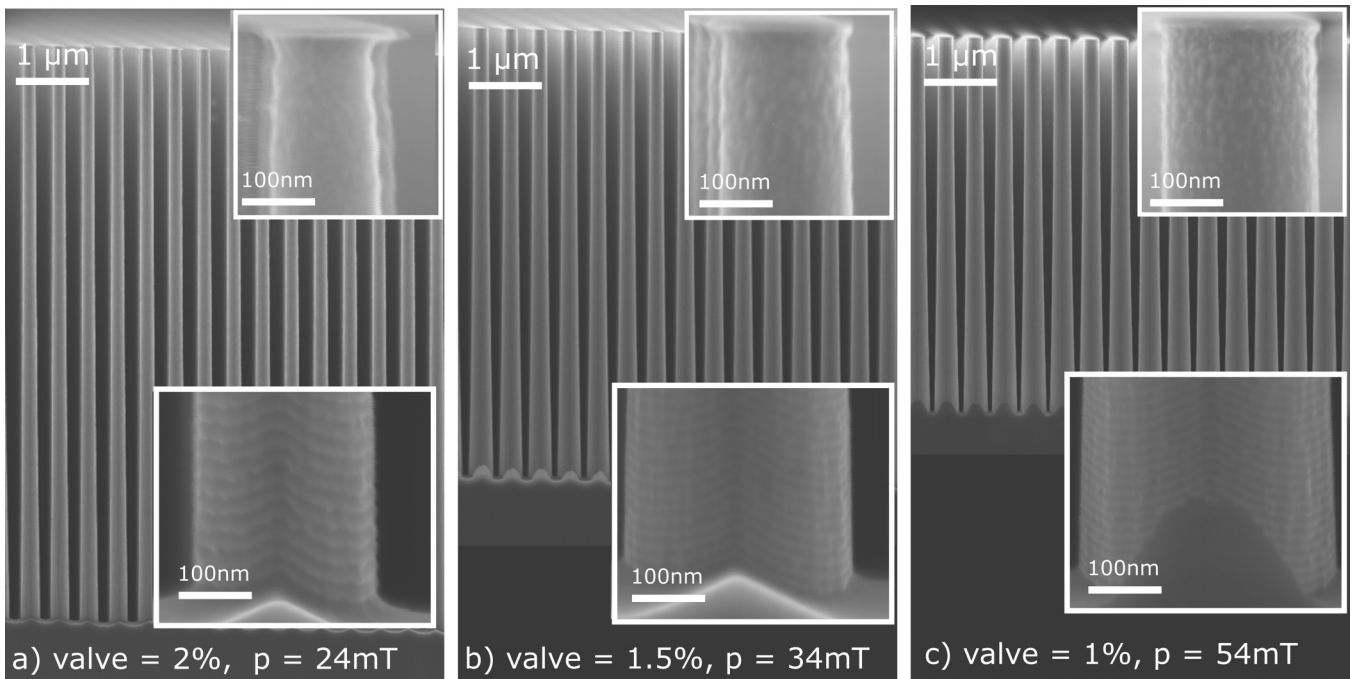
that the etch rate decreases with increasing pressure and the etch profile becomes more positive. The etch rate decreases because at a fixed plasma power, the increased pressure will increase the number of collisions between electrons and  $\text{SF}_6$  molecules (the so-called collision frequency). Because the plasma is operating in the power-limited regime, the higher collision rate will lower the electron temperature  $T_e$ . This will result in less dissociation of  $\text{SF}_6$  molecules, and consequently, the etch rate will decrease. Again, the mask erosion is not affected as the R-step is unchanged. Thus, the selectivity will be lower when the pressure is increased.

## 3. E-flow

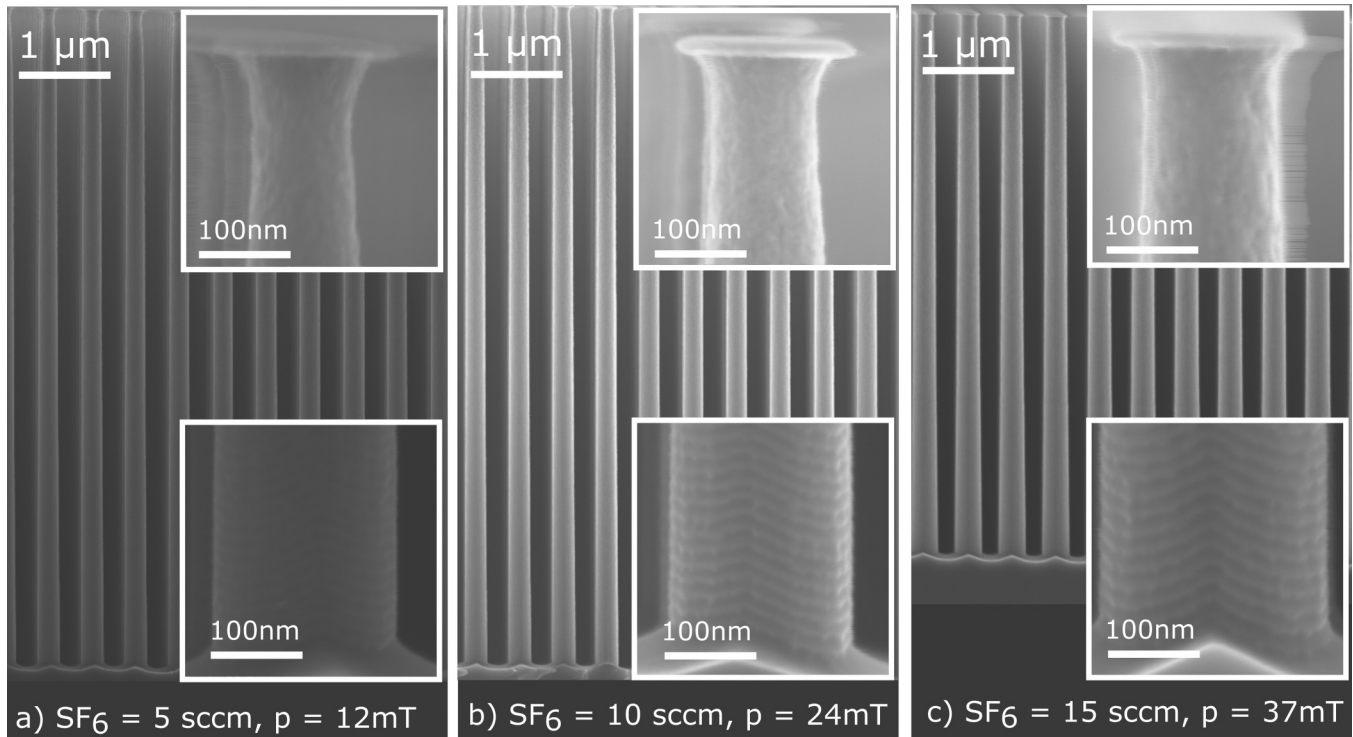
Finally, the power  $P_E$  is fixed at 10 W, and the valve position is fixed at 2%. Then, the  $\text{SF}_6$  flow is increased from 5 to 15 SCCM. Due to the fixed valve position, the pressure increases from 12 to 37 mTorr. As shown in Fig. 7, the etch profiles at 5 SCCM [Fig. 7(a)] and 10 SCCM [Fig. 7(b)] are deeper and straighter compared to that of 15 SCCM [Fig. 7(c)]. We already found that the plasma operates in the power-limited regime in which a higher  $\text{SF}_6$  flow will marginally contribute to a higher etch rate. Instead, a higher  $\text{SF}_6$  flow at a fixed valve position will increase the pressure in the reaction chamber. Therefore, as explained in Sec. III C 2, the electron temperature  $T_e$  will be lower, and both the etch rate and mask selectivity will drop when the flow is increased.



**FIG. 5.** Effect of changing the E-power on the etch profile at 15 SCCM  $SF_6$  flow and 2% valve (and 36 mTorr).



**FIG. 6.** Effect of changing the E-pressure on the etch profile at 10 SCCM  $SF_6$  flow and 15 W power.



**FIG. 7.** Effect of changing the SF<sub>6</sub> flow on the etch profile at 10 W power and 2% valve position.

#### D. Effect of total etch time

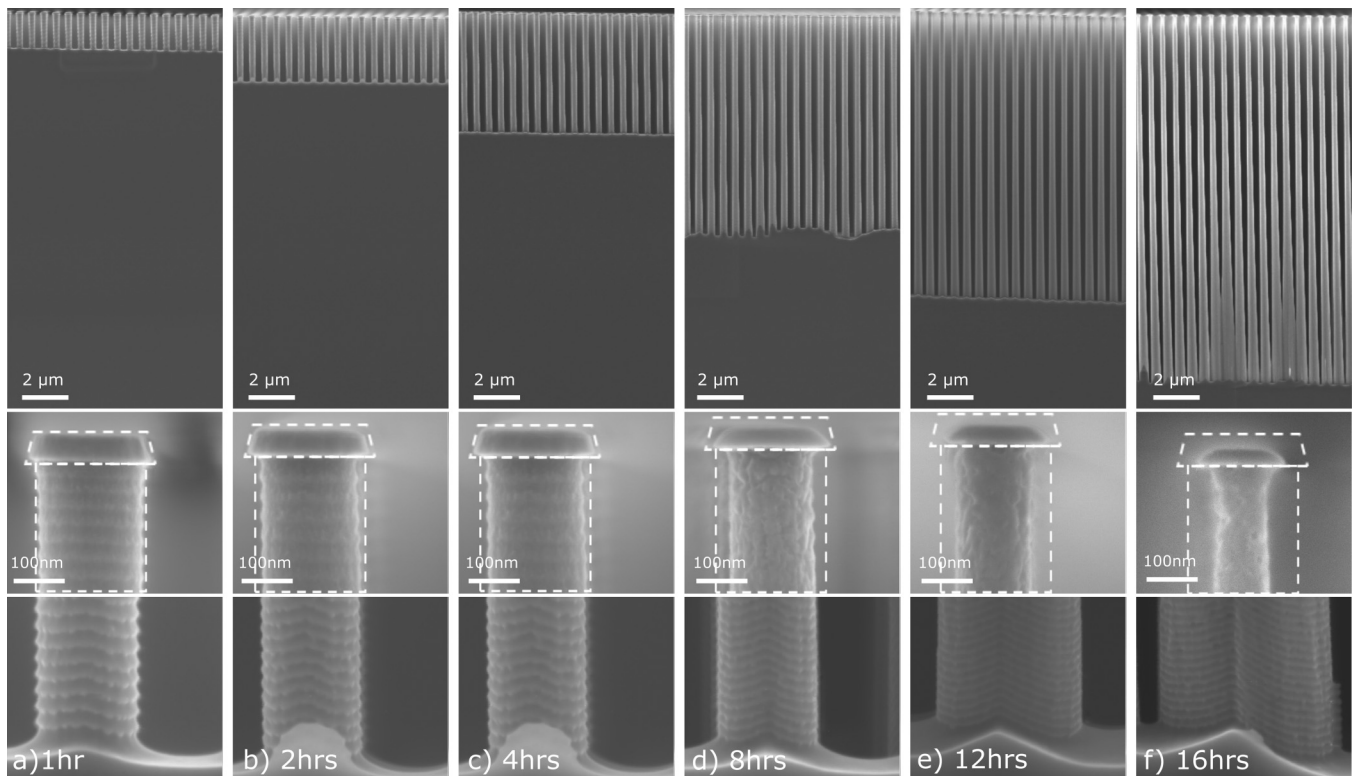
In Secs. III A–III C, the effect of some CORE parameters on the etch rate and profile of pillars has been investigated. In Secs. III D–III E, the main goal is to create pillars as high as possible with low undercut using the knowhow already gained. In the chosen CORE recipe, the O-step is improved for a strong protection of the silicon sidewall, especially at the top part of the etching pillar. Subsequently, the R-step is carefully tuned to straighten the profile with minimum mask erosion. The E-parameters are chosen such that a reasonable etch rate and small scallop size are formed. Then, samples are etched for increasing time. After 1 h [Fig. 8(a)], the etch pillars are 1.1 μm high and slightly negative tapered. After 2 h [Fig. 8(b)], the pillars are 2.1 μm high and almost perfectly straight. 4 h of etching [Fig. 8(c)] results in 3.9 μm etch depth with a slightly positive slope. 8 h [Fig. 8(d)] gives 7.1 μm etch depth and a more positive slope. 12 h [Fig. 8(e)] results in a height of 9.5 μm and an even more positive slope. Finally, 16 h [Fig. 8(f)] results in a height of 12.0 μm and the most positive slope. It is observed that the topside of the pillars becomes thinner with increasing etch time. This is because they are continuously being exposed to fluorine radicals. These radicals slowly and steadily etch the oxide passivation away. In addition, the pillar diameter at the bottom increases with time probably due to a decrease in the etch rate caused by RIE lag.<sup>42–45</sup> These observations are causing the pillar profile to become more positive. So, the total etch time has a

pronounced impact on the slope of the pillars and should be considered in order to get the highest possible aspect ratio. Furthermore, the erosion of the mask is remarkable. The first 8 h, the erosion rate is closely following the expected 2 nm/h. But after that the erosion rate drops strongly: between 8 and 12 h, it slows down to 1.25 nm/h, and between 12 and 16 h, it becomes only 0.25 nm/h. The authors have no explanation for this. Moreover, the chromium mask is not only getting thinner with etch time but also the diameter of the deposited dots decreases while etching. This phenomenon is similar to the photoresist in which the mask is retracting during the CORE etching process.<sup>18,46–48</sup> This retraction will have consequences for ultra-HAR processing, and therefore, this subject is studied in Sec. III F.

#### E. Ultra-HAR silicon etching

Since the CORE sequence has proper design rules, it makes the fine-tuning for ultra-HAR silicon structures easier and less time consuming than, e.g., the FC-based DREM procedure.<sup>49–53</sup> For instance, given the results presented in Fig. 8 and knowing the effect of the CORE parameters, the recipe was fine-tuned to get ultra-HAR features with straight and smooth sidewalls. More precisely, the recipe of Fig. 8 has been further improved by increasing the O-time to 8 s. This reduces the lateral etch while improving the self-limitation property. In addition, the R-power is increased from 25 to 35 W to ensure a straight profile. The ultra-HAR parameters





**FIG. 8.** Evolution of ultra-HAR silicon pillars while increasing the total etch time.

are found in Table II. As shown in Fig. 9(a), an array of 200 nm pillars with 400 nm periodicity is etched to a height of 11.4 μm. This corresponds to an aspect ratio of 57. The blurry parts of the zoom-in at the topside of the pillars [Fig. 9(b)] are believed to be due to local charging of the ultra-HAR pillars making them to vibrate during scanning.

To demonstrate the ability of the CORE sequence to fabricate sub-100 nm HAR features, samples with 60 nm dots created by e-beam and lift-off are used. The pillars in Fig. 9(c) are correctly shaped except for the top part as shown in Fig. 9(d), which is positive tapered. The positive taper is believed to be induced by chromium retraction as described in Sec. III D that has become severe

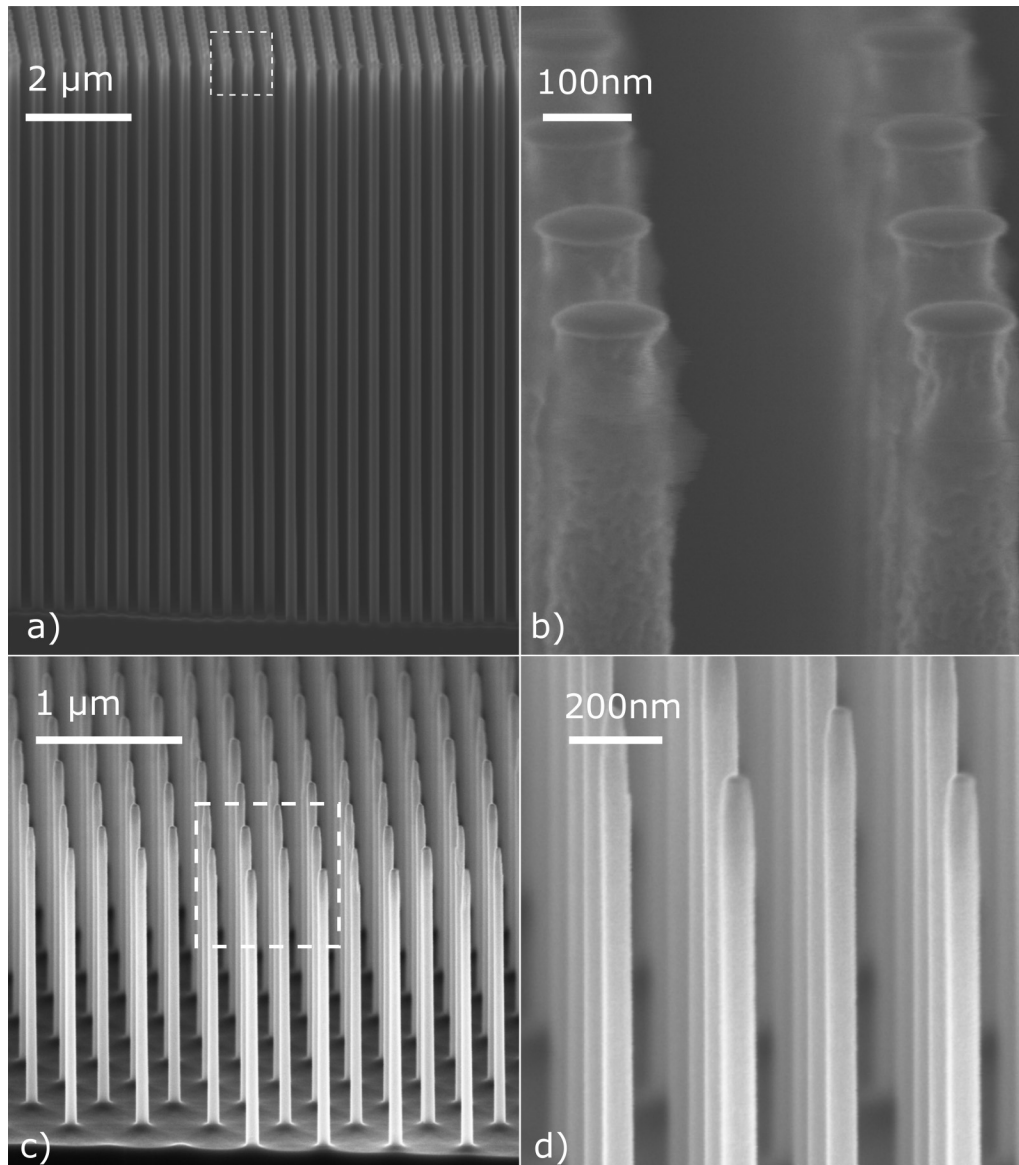
**TABLE II.** Ultra-HAR CORE recipe for nanoscale silicon etching.

CORE	C	O	R	E
Time (s)	4	8	16	84
Pressure (mT)	0.8	50	0.2	36
O <sub>2</sub> (SCCM)	50	50	0	0
Platen power (W)	0	15	35	15
DC self-bias (V)	0	0	100	0
SF <sub>6</sub> (SCCM)	0	0	5	10

at the end of the pillar etch process. Consequently, the retraction will be transferred into the silicon and causes profile distortion. This restricts the maximum achievable aspect ratio. The distortion can be reduced by improving the mask topography (e.g., by optimizing the lift-off procedure).

### F. Chromium mask etching and retraction

In Secs. III D–III E, we have found that chromium is retracting substantially while performing CORE etching. To find out the cause, a specific sample is created. The sample consists of a silicon wafer with a layer of chromium and on top of that is a layer of polysilicon. Subsequently, stepper lithography is used to form 200 nm holes with 400 nm periodicity. This resist pattern is transferred into the polysilicon layer using the CORE sequence and will stop on the chromium layer. Finally, the sample is placed in a plasma oxygen system and ashed for 20 min with 400 SCCM O<sub>2</sub> flow at 1 Torr and 1000 W power. During ashing, the temperature quickly raises from room temperature up to almost 200 °C. The result is shown in Fig. 10(a). Evidently, the resist is stripped totally, but it is also observed that the sandwiched chromium layer is undercutting the polysilicon top-layer isotropically by ~250 nm and leaving a free-hanging polysilicon membrane. Additional experiments revealed that the chromium isotropic erosion rate is highly dependent on



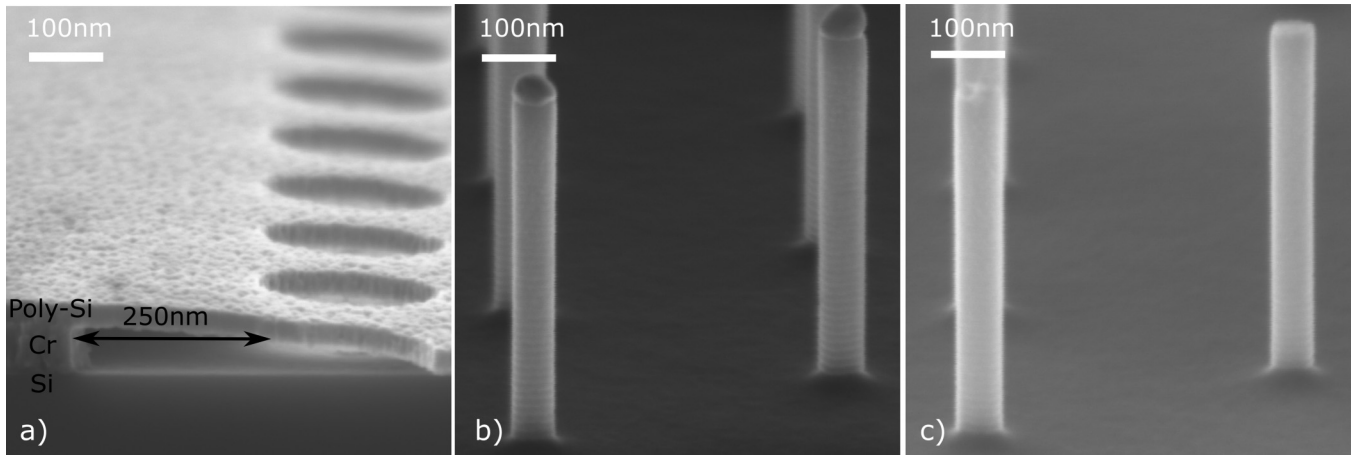
**FIG. 9.** (a) Ultra-HAR 200 nm diameter silicon pillars etched by the CORE recipe. (b) The blurry imaging at the topside might be due to “pillar vibration” by the locally charging scanning electron beam. (c) 60 nm diameter pillars derived from e-beam lithography. (d) The positive taper at the topside is believed to be due to chromium retraction during CORE etching.

the temperature and applied power during plasma ashing.<sup>35–38</sup> Below 100 °C, almost no erosion is observed and the erosion is only substantial at the maximum power. Nitrogen or CF<sub>4</sub> plasmas do not attack chromium; only O<sub>2</sub> supports ashing. Therefore, it is assumed that the erosion is due to volatile CrO<sub>x</sub> species. The above experiment shows that chromium can be an appropriate sacrificial layer for surface micromachining, because sticking of movable parts of nano- or microdevices during wet etching is avoided.<sup>53–55</sup> The isotropic etch behavior of the chromium layer is exploited to

remove it from the 60 nm diameter pillars as presented in Fig. 10(b) (before ashing) and Fig. 10(c) (after ashing).

### G. Effect of the carrier wafer

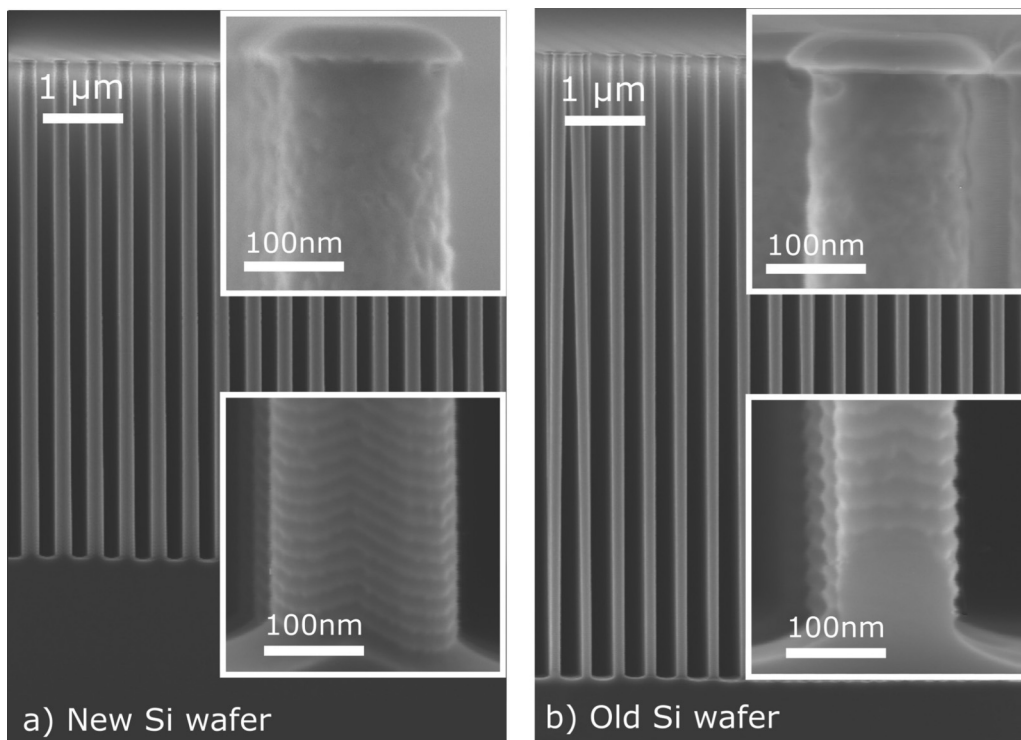
Additional experiments have been carried out to examine the impact of the surface condition of the silicon carrier wafer on the etch result. The first sample is attached to a new polished wafer [Fig. 11(a)], and another sample is attached to a used wafer



**FIG. 10.** Chromium etching in a plasma ash system. (a) Isotropic undercutting of a polysilicon membrane. (b) 60 nm e-beam defined pillars before chromium removal. (c) The same pillars after chromium removal.

[Fig. 11(b)]. The latter has been used several times and has started to become rough and blackened. The consequence of a roughened carrier wafer with respect to a polished wafer is that the etch rate of this carrier wafer is lower, and therefore, the fluorine concentration

inside the reactor will be higher. As a result, the etch rate of a sample attached to a roughened wafer increases and the etch profile becomes less positive tapered with respect to a sample attached to a new wafer.



**FIG. 11.** Effect of the carrier wafer on the etch profile. (a) A new wafer and (b) a roughened wafer.

#### IV. CONCLUSIONS

This study demonstrated a process to fabricate ultra-HAR silicon pillars using a chromium mask and the CORE sequence. The influence of various CORE parameters has been carefully investigated and optimized with respect to low mask undercut, high directionality, and highest achievable aspect ratio. Using the optimal parameter setting in which all the CORE steps are well balanced, the fabricated pillars have smooth and straight sidewalls with a low undercut. In general, a stronger oxidation will improve silicon surface passivation and step coverage. The latter is because the plasma oxidation is diffusion controlled and, therefore, the growing oxide film will limit the oxide growth at about 3 nm. Therefore, after sufficient oxidation, all surfaces including ultra-HAR features tend to have the same protection. The subsequent R-step controls the directionality and should be just enough to fully remove the horizontal surfaces from the grown oxide, but it should be limited to prevent too much mask erosion. The following E-step is able to control the scallop size and the slope profile, the longer the E-step the less positive the slope will become. However, the E-step should be taken not too long in order not to penetrate the sidewall protection and to cause sidewall roughness. In addition, the strength of the E-step (i.e., the amount of silicon etched per cycle) is affected by the E-pressure and flow, but the effect depends on the specific parameter choice (i.e., if it is operating in the power-limited or flow-limited regime). Furthermore, RIE lag in HAR features will weaken the E-step and, thus, make the scallops smaller and the profile more positive.

To summarize the CORE sequence: A stronger oxidation step, whether due to more O-time or O-power, will result in less mask undercut and in a more positive taper. A stronger removal step, whether due to more R-time or R-power, will result in stronger mask erosion and in a less positive taper. A stronger E-step, whether due to more E-time or E-power, will result in bigger scallop size and a less positive taper. Finally, the chromium mask has proven to be an appropriate candidate to etch silicon with a selectivity of up to 500. Using 60 nm of chromium, the aspect ratio of the pillar gaps has been tuned beyond 55, and the pillars itself could reach 200. This is believed to be further improvable when a thicker mask is used.

#### ACKNOWLEDGMENTS

The author would like to thank the DTU Nanolab staff for instrument support. Specifically, the authors thank Matthias Keil for support with DUV lithography, Peixiong Shi for support with e-beam lithography, and Roy Cork and Martin Nørvang Kristensen for the technical support with plasma etching processes.

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