| Process flow title | | | Revision |
|---|---|---|---|
| **DTU Nanolab - Solar cell process** | | | **2.6** |
| **DTU Nanolab**<br>National Centre for Nano Fabrication and Characterization | Contact email<br>jehan@dtu.dk<br>kabi@dtu.dk<br>mmat@dtu.dk | Contact persons<br>Jesper Hanberg<br>Karen Birkelund<br>Maria Matschuk | Contact phone<br>45255828<br>452556436<br>452555723 |
| | Labmanager group<br>- | Batch name<br>May 2024 | Date of creation<br>24 May 2016 | Date of revision<br>13-Jan-25 |

## Objective

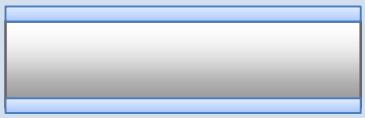
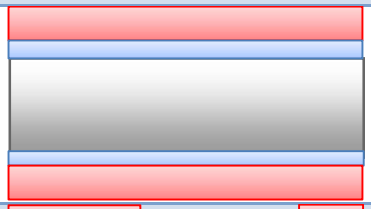
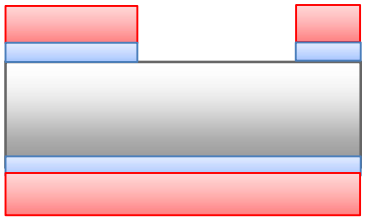
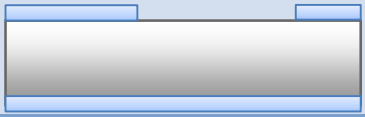
This process was originally used in the UV-lithography Green Belt course organized by DTU Nanolab (in 2016). This is an updated version (April 2024). The purpose is to provide an example process flow and to educate Cleanroom users in general UV-lithographic techniques. The outcome are test wafers with solar cells.

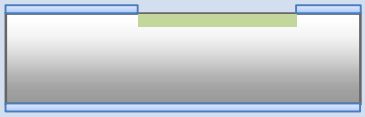
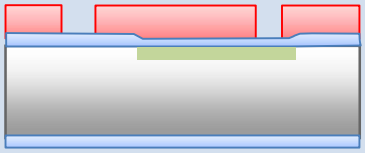
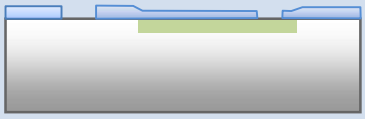
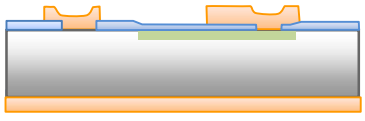
## Substrates

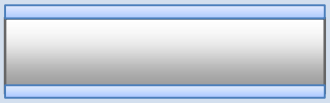
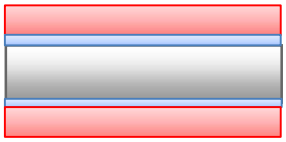
| Substrate | **Orient.** | **Size** | **Doping/type** | **Polish** | **thickness** | **Box** | **Purpose** | **#** | **Sample ID** |
|---|---|---|---|---|---|---|---|---|---|
| Silicon | <100> | 4” | p(Boron) | SSP | 525±25µm | | Device wafers | 6 | S1-S6 |
| Silicon | <100> | 4” | p (Boron) | SSP | 525±25µm | | Test wafers | 4 | T1-T4 |
| Silicon | <100> | 4” | p (Boron) | SSP | 525±25µm | | Dummy wafers | 2 | D1-D3 |

* Test wafers: T1-T4 used for quality control (measurements) in between process steps
Dummy wafers: D1-D3 are used to measure furnace performance (from RCA shelf)
Other dummy wafers: need to be purchased and can be used (if wanted) to improve the uniformity in furnace processes

## Figures

| Figure | **Caption** | **Step** | **Figure** |
|---|---|---|---|
| 1 | After SiO2 oxidation | 1.2 |  |
| 2 | After Spin coating | 2.3 |  |
| 3 | After UV lithography (mask layer 1: N+ doped area) | 2.5 |  |
| 4 | After SiO2 etch in BHF | 3.1 |  |
| 5 | After Strip resist | 3.4 |  |

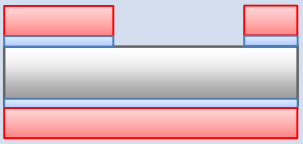
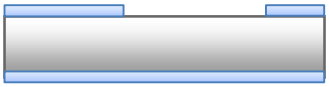
| | | | |
|---|---|---|---|
| 6 | After Phosphor predep | 4.2 |  |
| 7 | After SiO2 etch in BHF | 4.3 |  |
| 8 | After thermal oxidation of SiO2 | 4.5 |  |
| 9 | After UV lithography (mask layer 2: contacts) | 6.3 |  |
| 10 | After SiO2 etch in BHF | 7.2 |  |
| 11 | After resist strip | 7.4 |  |
| 12 | After lithography (mask layer 3: metal) | 8.4 |  |
| 13 | After metal deposition | 9.2 |  |
| 14 | After lift-off | 9.34 |  |

| Step | Heading | Equipment | Procedure | Comments |
|---|---|---|---|---|
| **1** | **$SiO_2$ Dry Oxidation**<br>*(Creating SiO2 protection layer (and insulator/protection) for areas not to be doped)* | | | **Wafer S1-S6, T1-T3, D1 from Nanolab, 2 dummy wafer** |
| 1.1 | RCA clean | RCA bench | Follow standard procedure. | All wafers, incl dummies need to be RCA cleaned |
| 1.2 | $SiO_2$ dry oxidation | Boron Drive-in (A1) | Place D1 in the center of the boat and place device and test wafers equally distributed on each side of D1. No spacing between wafers. Place two dummy wafer on each side outermost (to improve uniformity).<br>*Target thickness: 150±10nm*<br><br>*Recipe: Dry1050*<br>*Oxidation time: 170 min*<br>*Anneal: 20 min* |  |
| 1.3 | Inspection | FilmTek 4000 (or Ellipsometer) | Measure oxide thickness on both dummies and D1.<br>*Target thickness: 150±10 nm* | Note in measurement sheet. Fill out furnace A1-logbook (with D1). |
| **2** | **UV Lithography– 1.5µm AZ5214E**<br>*(Create mask for doping of active areas)* | | | **Wafer S1-S6** |
| 2.1 | Surface treatment | Oven HMDS-2 | Coat all wafers with HMDS<br><br>*Recipe: program 01*<br>*Time: ca. 30 min* | |
| 2.2 | Spin Coating - **backside** - | Spin Coater: UV Gamma | Coat backside of the device wafers with 1.5 µm AZ 5214E resist<br><br>*Recipe: 3412 DCH 100 mm AZ 5214E 1.5 µm prox bake*<br>*Spin-off time: 50-60 s*<br>*Soft Bake Temp: 100°C (proximity)*<br>*Soft-Bake time: 65 sec*<br>*without HMDS* | Check Spinner nozzle and clean with dummy wafer (if required) |
| 2.3 | Spin Coating - **frontside** - | Spin Coater: UV Gamma | Coat frontside of the device wafers with 1.5 µm AZ5214E resist<br><br>*Recipe: 3412 DCH 100 mm AZ 5214E 1.5 µm prox bake*<br>*Spin-off time: 50-60 s*<br>*Soft Bake Temp: 100°C (proximity)*<br>*Soft-Bake time: 65 sec*<br>*without HMDS* |  |
| 2.4 | Exposure | Maskless Aligner 3 (MLA-3) | **Mask layer: "layer 1 - N+ doped areas"**<br><br>*Mode: Quality (ca. 15-25 min), Fast (8-10 min)*<br>*Dose: 105 mJ/cm2*<br>*Defocus: 2*<br>*Laser: 375 nm* | *Note: 405 nm require increased dose; dose and defoc not very critical for solar cell design itself*<br><br>*MA6 Aligner: mask: "n+ doped", Alignment to marks on wafer, Hard contact, duration: 5 sec* |
| 2.5 | Develop | TMAH UV-lithography | Develop exposed resist in TMAH<br><br>*Recipe: 1002 DCH 100 mm SP60s*<br>*Dev time: 60 s* |  |
| 2.6 | Inspection | Optical microscope | Check pattern and alignment marks | |

## 3 $SiO_2$ Wet Etch

*(Remove $SiO_2$ in unmasked areas (areas to be doped))*

**Wafer S1-S6**

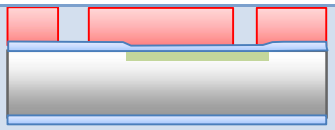
| | | | | |
|---|---|---|---|---|
| 3.1 | $SiO_2$ etch | Oxide etch 2: BHF (Wet bench 04) | Etch $SiO_2$ in exposed areas in BHF. Etching rate: 75-80 nm/min. Rinse in DI water.<br><br>*Etch time: 2-2½ min*<br>*DI rinse: 5 min ± 30 sec* |  |
| 3.2 | Drying | Spin dryer | Transfer wafer box into spin dryer | |
| 3.3 | Inspection | Optical microscope | Check pattern and alignment marks | |
| 3.4 | Strip resist | Plasma Asher 4 (Resist Strip) | *Recipe: 18*<br>*Time: 30 min*<br>*O2 flow: 400*<br>*N2 flow: 70*<br>*Power: 1000 W* | *Alternative Resist Strip: 10 min*<br>  |
| 3.5 | Inspection | Dektak XTA | Measure step height of one or two device wafers<br>Target: 150±10 nm | **Wafer S1-S6**<br>Note in measurement sheet |

## 4 Phosphor Doping

*(Doping with phosphor - silicon in "open areas")*

**Wafer S1-S6, T1-T4, D2-D3 from Nanolab, 2 dummy wafer**

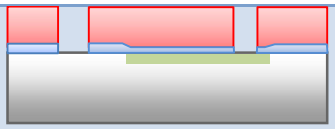
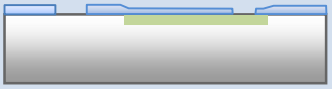
| | | | | |
|---|---|---|---|---|
| 4.1 | RCA clean | RCA bench | Follow standard procedure but **without HF dip**.<br>All wafers, incl dummies need to be RCA cleaned | **Wafer S1-S6, T1-T4, D2-D3, 4 dummy wafer**<br>(D2 for A4-furnace, D3 for A3-furnace)<br>No HF<br>*RCA clean 4 dummy wafers for A4 (2) and A3 (4). Dummies from A4 can be re-used for A3.* |
| 4.2 | Phosphor doping (gas: $POCl_3$) | Furnace: Phosphorus Predep (A4) | Place D2 in the center of the boat and place device and test wafers equally distributed on each side of D2. No spacing between wafers. Front-side to the left. Place one new dummy wafer on each side outermost to device wafers (to prevent unintended doping from "used" dummy). Place two dummy wafers on each side outmost (to improve uniformity).<br><br>Target doping : $R_{sheet}$=40 Ω/²<br><br>*Recipe: POCL950*<br>*Time: 15 min*<br>*Anneal: 20 min* | **Wafer S1-S6, T1, T4, D2, 2 dummy wafers**<br><br>Note diffusion time in furnace A4-logbook<br>  |
| 4.3 | Measure resistivity | 4 Point Probe | Measure resistivity on D2 | Note in measurement sheet. Fill out furnace A4-logbook (with D2). |
| 4.4 | Etch of phosphor glass | BHF in RCA bench for doped wafers | Removes all phosphor glass and only some of the dry oxide.<br><br>*Time: exactly 30 sec* | **Wafer S1-S6, T1, T2**<br><br>*Note that the wafer becomes hydrophobic.*<br>  |

| | | | | |
|---|---|---|---|---|
| 4.5 | Inspection | FilmTek 4000 (alt. Ellipsometer) | Measure remaining oxide thickness of T1 and T2 and calculate how much Phosphorglass/doped SiO2 and SiO2 has been etched.<br>Target thickness: 150 – 70 ±10 nm | Note in measurement sheet. |
| **5** | **$SiO_2$ Dry Oxidation**<br>*(Creating SiO2 insulation layer)* | | | **Wafer S1-S6, T3, T4, D3** |
| 5.1 | $SiO_2$ dry oxidation | Phosphor Drive-in (A3) | Place D3 in the center of the boat and place device and test wafers equally distributed on each side of D3. Front-side to the left. No spacing between wafers. Place two dummy wafer on each side outermost (to improve uniformity).<br>Target thickness: 90 ±10nm<br>*Recipe: Dry1050*<br>*Oxidation time: 75 min*<br>*Anneal: 20 min* | **Wafer S1-S2, T3, T4, D3, 2 dummy wafers**<br>Note result in the furnace log (D2) and in measurement sheet.<br>  |
| 5.2 | Inspection | FilmTek 4000 (Ellipsometer) | Measure oxide final thickness.<br>Target thickness: 90 ±10 nm (dummy D3)<br>T3 (80+90 ±10 nm)<br>T4 (ca. 90 ±10 nm) | Fill out A3-furnace logbook.<br>*Note: This measurement cannot be done between both furnaces (A4 and A3), else another RCA is required.* |
| 5.3 | Measure resistivity | 4 Point Probe | Measure resistivity on T4 | Note in measurement sheet |
| **6** | **UV Lithography – 1.5µm AZ5214E**<br>*(Create mask for etching of SiO2 to open "free access" to silicon for metal contacts)* | | | **Wafer S1-S6** |
| 6.1 | Spin Coating - frontside - | Spin Coater: Gamma UV | Coat the wafers with 1.5 µm positive resist AZ5214E (Spin-off: 30-60 s; Soft Bake at Temp: 90°C, time: 90 sec)<br>*Recipe: 3411 DCH 100mm 5214E 1.5um HMDS*<br>*Spin-off time: 55 s*<br>*Soft Bake Temp: 100°C (proximity)*<br>*Soft-Bake time: 65 sec*<br>*without HMDS* | |
| 6.2 | Exposure | Maskless Aligner MLA-3 (MLA-2, MA-6) | **Mask layer: "layer 2 - contacts"**<br>*Mode: Quality (ca. 20-25 min), Fast (4-7 min)*<br>*Dose: 105 mJ/cm2*<br>*Defocus: 2*<br>*Laser: 375 nm*<br>*Alignment: check location for alignment marks in design file* | *Note: 405 nm requires increased dose*<br>*MA6 Aligner: mask: "contacts", Alignment to marks on wafer, Hard contact, duration: 5 sec* |
| 6.3 | Develop | Developer: TMAH UV-Lithography | Develop in TMAH<br>Recipe: *1002 DCH 100 mm SP60s*<br>*Dev time: 60 s* |  |
| 6.4 | Inspection | Optical microscope | Check pattern and alignment | |

## 7 $SiO_2$ Wet Etch

**Wafer S1-S6**

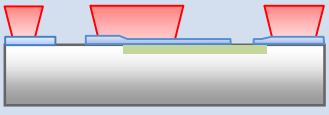
*(Etching of SiO2 to open "free access" to silicon for metal contacts)*

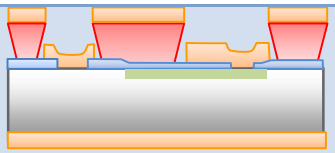
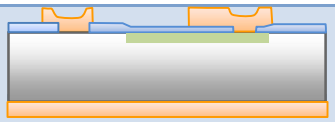
| | | | | |
|---|---|---|---|---|
| 7.1 | SiO-etch | Oxide etch 2: BHF | Etch $SiO_2$ in exposed areas in BHF. Etching rate: 75-80 nm/min. Rinse in DI water.<br><br>*Etch time: 2-2½ min*<br>*DI rinse: 5 min ± 30 sec* | Note that the backside becomes hydrophobic. |
| 7.2 | Drying | Spin dryer | Transfer wafer box into spin dryer |  |
| 7.3 | Inspection | Optical microscope | Check pattern and alignment | |
| 7.4 | Strip resist | Plasma Asher 2 | *Recipe: 18*<br>*Time: 30 min*<br>*O2 flow: 400*<br>*N2 flow: 70*<br>*Power: 1000 W* |  |
| 7.5 | Inspection | Dektak XTA | Measure step height between Si-P (N+) and SiO2 on device wafers<br>Target: 90±10 nm in N+ areas<br>Target: 130±10 nm in un-doped areas | |

## 8 Lithography – 2.0µm n-LOF2020

**Wafer S1-S6**

*(Create mask for deposition and lift-off for metal contacts)*

| | | | | |
|---|---|---|---|---|
| 8.1 | Coat Wafers | Spin Coater: Gamma UV | Coat the wafers with 2.0 µm negative resist nLOF 2020<br>*Recipe: 2420 - DCH 100mm nLOF 2020 2 um*<br>*Soft Bake temp: 110°C*<br>*Soft Bake time: 60 sec* | |
| 8.2 | Transport of wafers | non-transparent transport box | Transport wafers inside a black or blue transport box | To avoid unwanted exposure from the white light in the cleanroom. |
| 8.3 | Exposure | MLA-2<br>(MA-6) | **Mask layer: "layer 3 - metal"**<br><br>*Mode: Quality (ca. 45 min), Fast (ca. 20-25 min)*<br>*Dose: 550 mJ/cm2*<br>*Defocus: 0*<br>*Laser: 375 nm (!)*<br>*Alignment: check location for alignment marks in design file* | *Note: nLof 2020 requires MLA-2 due to wavelength;*<br><br>*MA6 Aligner: mask: "metal", Alignment to marks on wafer, Hard contact, duration: 5 sec* |
| 8.4 | Post Exposure Bake and Develop | Developer: TMAH UV-Lithography | Post Exposure Bake and Development<br><br>*Recipe: 3001 DCH 100mm PEB60s@110C+SP60s*<br>*PEB temp: 110°C*<br>*PEB time: 60 sec;*<br>*Dev time: 60 s* | Fill out the logbook.<br>  |
| 8.5 | Inspection | Optical microscope | Alignment check | |

| | | | | |
|---|---|---|---|---|
| **9** | **Aluminum pattern**<br>*(Deposition of metal contacts)* | | | **Wafer S1-S6** |
| 9.1 | Aluminum deposition<br>- frontside - | E-Beam Evaporator (Temescal) | Deposition of Titanium and Aluminum on front side<br><br>*Thickness: 50 nm Ti + 300 nm Al* | Titanium acts as barrier layer to avoid diffusion of aluminum into silicon |
| 9.2 | Aluminum deposition<br>- backside - | E-Beam Evaporator - 10 pockets | Deposition of Aluminum on back side<br><br>*Thickness: 300 nm Al* |  |
| 9.3 | Lift-off | Lift-off (D-3) | Remove resist using Remover 1165 for 2-3 min. Temperature: 45 °C. Start the ultrasound for 10 min. Rotate wafers and start ultrasound for another 10 min. Rinse in DI water for 5 min (300±30 sec). | Fill out the logbook. |
| 9.4 | Drying | Spin dryer | Transfer wafer box in dedicated transport box (single green or yellow dots) into spin dryer |  |
| 9.5 | Inspection | Optical microscope | Check for complete lift-off | |
| 9.6 | Annealing | Furnace: Al Anneal (C4) | Anneal wafers for 15min at Temp: 400 °C<br>*Recipe: ANN400* | Fill out the logbook. |
| 9.7 | Inspection | Dektak | Measure thicknesses (on front and back). | |
| 9.8 | Inspection | 4 Point Probe | Measure metal sheet resistance on backside. | |

## Alignment Marks