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| Objective |
| Batch name: Process template |
| This process flow is a guideline on how to spin coat, expose, and develop AZ 5214E positive on a chip mounted on a 100 mm carrier wafer, using automatic spin coater, maskless aligner and automatic developer.This is an example process flow to be used as a template. It should contain:* The objective of the process
* Substrates/samples used in the flow - both actual samples to be processed (device wafers) and any monitor samples for the different process steps
* The Process flow main processes and steps
* Recommended: Figures illustrating the sample before and after each main process step

How to use this template (works only with the .dotx template file):* Fill out the fields in the header
* Add process steps by using Quick Parts under Insert (your cursor should be located at the beginning of the next (empty) step)Select the “Process Step” item
* Other document parts can be inserted the same way: Substrates, Figures, etc.
* The Content (TOC) on the last page is an option, but provides a nice overview for very long process flows
 |

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| --- |
| Substrates |
| Substrate | Orient. | Size | Doping/type | Polish | thickness | Box | Purpose | # | Sample ID |
| Silicon  | <100> | 100 mm | n (Phos.) | SSP | 525 ±25 µm |  | Device wafers | 2 | S1-S2 |
| Silicon  | <100> | 100 mm | n (Phos.) | SSP | 525 ±25 µm |  | Test wafers | 1 | T1 |

Comments: Number of wafers is for illustration only

|  |
| --- |
| Figures |
| Figure | Caption | Step | Figure |
|  | After SiO2 depNot part of this process flow example | 2.1 |  |
|  | After lithography | 3.5 |  |
|  | After BHF etchNot part of this process flow example | 4.1 |  |
|  | After resist stripNot part of this process flow example | 4.4 |  |
|  | After lithographyNot part of this process flow example | 5.6 |  |
|  | After metal depositionNot part of this process flow example | 6.1 |  |
|  | After lift-offNot part of this process flow example | 6.2 |  |

Comments:Click here to enter text.

|  |  |  |  |
| --- | --- | --- | --- |
| Step Heading | Equipment | Procedure | Comments |
| 1. Preparation
 | **All wafers** |
| * 1. Wafer selection
 | Wafer box | Take the wafers from the storage and put them in a wafer box.  | Note the wafer IDs in the batch traveler |
| 1. SiO2 deposition
 | **All wafers** |
| * 1. Not part of this process flow example
 |  |  |  |
| 1. Lithography – standard
 | **All wafers** |
| * 1. Surface treatment
 | Oven: HMDS – 2 | HMDS treatment for Si, SiO2, and Borofloat**Recipe:** 01 | HMDS priming *cannot* be done on Gamma spin coaters with crystal bonded substrates |
| * 1. Bond chip to carrier
 | Hotplate | Use crystal bondThe chip must be in the center of the carrier wafer |  |
| * 1. Coat wafers
 | Spin Coater: Gamma UV*Or*Spin coater:Gamma e-beam & UV | **Resist:** AZ 5214E**Spin:**30 s @ 4500 rpm (for 1.5 µm)**Softbake:**60 s @ 90 °C**Sequence gamma UV:**3410 DCH 100mm AZ5214E 1.5um**Sequence gamma ebeam & UV:**4110 DCH 100mm AZ5214E 1.5um | **Remember:** No inline HMDS priming with crystal bonded substrates!Resist thickness can be measured on FilmTek or ellipsometer |
| * 1. Exposure
 | Aligner: MLA1*Or*MLA2*Or*MLA3 | **Design:**Your design file**Exposure dose:**MLA1: 80 mJ/cm2 MLA2: 65 mJ/cm2 (375 nm)MLA3: 65 mJ/cm2**Defocus:** MLA1: -4MLA2: 0 (optical AF)MLA3: -2 | Further information is available on labadviser:https://labadviser.nanolab.dtu.dk/index.php?title=Specific\_Process\_Knowledge/Lithography |
| * 1. Develop
 | Developer: TMAH UV-lithography | **Development in TMAH (AZ 726 MIF):** single puddle, 60 s**Sequence:**1002 DCH 100mm SP 60s | Consider long PEB if different resist is used, e.g. 2min @ 110°C for nLOF or MiR |
| * 1. Inspection
 | Optical microscope | Check pattern and alignment marks |  |
| * 1. De-bond chip
 | Hotplate | Remove chip from carrier and clean before continuing processing |  |
| 1. SiO2 etch
 | **All wafers** |
| * 1. Not part of this process flow example
 |  |  |  |
| 1. Lithography – Lift off
 | **All wafers** |
| * 1. Not part of this process flow example
 |  |  |  |
| 1. Aluminum pattern
 | **Only device wafers!!** |
| * 1. Not part of this process flow example
 |  |  |  |
| 1. Linewidth measurement
 | **All wafers** |
| * 1. Not part of this process flow example
 |  |  |  |

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