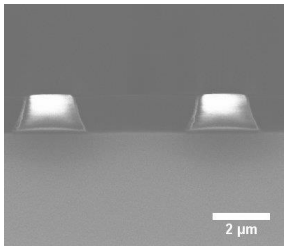
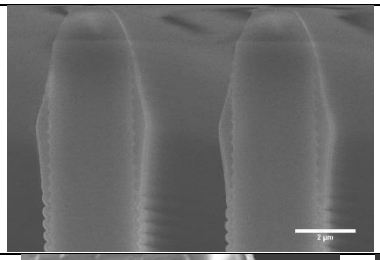
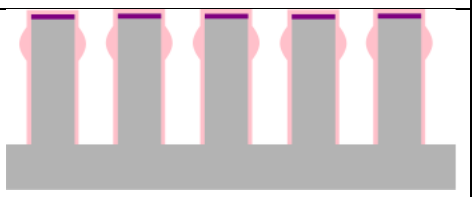
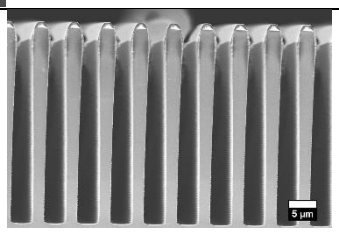
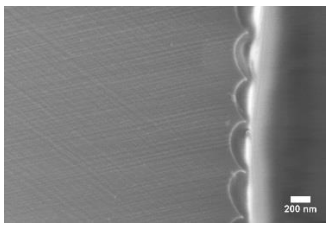
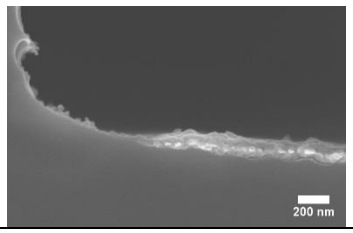
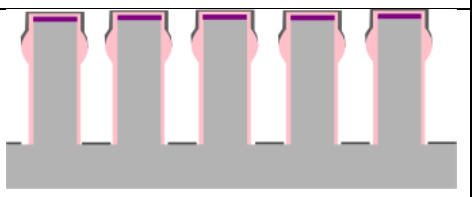
Process flow title			Revision
Gold plating in Si trenches with seed layer			**2.0**
DTU Nanolab Nationalt Center for Nanofabrikation og -karakterisering	Contact email chasil@.dtu.dk	Contact person Chantal Silvestre	Contact phone 52769482
	Group Silicon Technology / Batch name	Date of creation 25-04-17	Date of revision 28-02-20

Caption	Step	Figure
Resist patterning AZ5214e, 1.5um		
DRIE		
Metal deposition (thermal evaporation)	   	
Polymer removal		
Electroplating		

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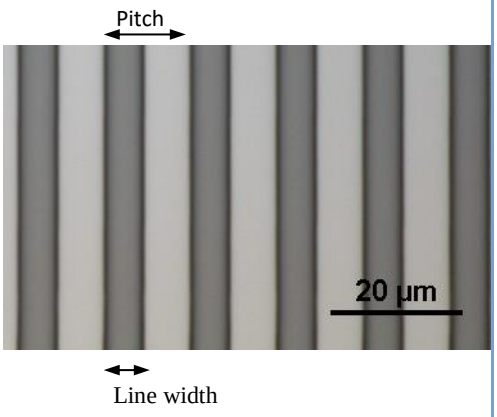
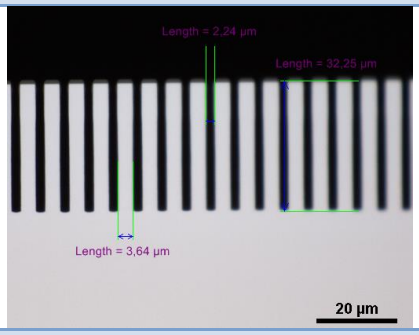
Gold plating in Si trenches with seed layer	**2.0**	28-02-2020	chasil@dtu.dk

Step	Heading	Equipment	Procedure	Comments
1	**Wafer selection**			
1.1	Wafer	Shelf	ON528 or ON516 n-type/Phosphor Resisitivy 1-20 Ωcm <100> DSP 350 ± 15 µm Price 283 DKK/pce	Remember to buy them in LM if you take the wafer from the shelf.
2	**Resist spinning**			
2.1	Spin resist	Gamma UV spin coater	AZ5214E 1.5um with HMDS	
2.2	Mask exposure	Maskless aligner	**Focus** : 0 **Dose** : 70 mW/cm^2 **Mask** : your own mask design	This recipe has been tested with line width from 3µm to 13µm
2.3	Develop	Developer: TMAH UV-lithography	**Development in TMAH**: single puddle, 60 s **Sequence:** DCH 100mm SP 60s	This is the development of the resist which has been exposed. After this step, the pattern is visible on the wafer.
3	**Characterization**			
3.1	Line width measurement	Microscope NIKON	Magnification 100x	Measure the line width and the line pitch with the magnification 100x. Remember to press on "Y" to print the scale and dimension on the image before saving the image. Move to magnification 100x step by step. On the image : light gray is Si and dark gray is resist 
4	**DRIE**			
4.1	Change temp. chuck	Pegasus	**Recipe :** change temp / temp -19C	We have a better control of the etch rate when temperature is low. Therefore, we run the dry etch at a chuck temperature of -19C Change temperature chuck to -19C
4.2	DRIE	Pegasus	**Recipe** : DREAM_3um **Number of cycle** : 100 cycles	DREAM_3 is described in my thesis. 3µm stands for the smallest dimension that recipe is made for. Smaller dimensions are not guarantee. Scallops size: ~300nn
4.3	Clean	Pegasus	Unload the wafer Run cleaning chamber Recipe : TDESC 20min	

5	**Characterization**			
5.1	Depth etch	Microscope NIKON	Cleave one of the test chip and place on cross-section holder in the microscope. Magnification 100x	
6	**Metallization – seed layer deposition**			
6.1	Metallization	Temescal	Ti : 10nm Au : 70nm	Use Temescal instead of Wordentec. The Wordentec has more scattering and the gold is not nicely placed in the bottom of the trench. Repeat same recipe on the back side for electroplating contact layer.
7	**Lift-off & Clean**			
7.1	Lift-off	Fumehood : lift-off	Beaker of acetone No ultrasound	Acetone bath until lift-off done (~7 min) Isopropanot bath for ~30 sec Rinse in DI water. **NOTE**: do not use ultra-sounds. It breaks the lines.
7.2	FC clean	Plasma asher 1	Oxigen plasma for 60 min Use recipe 99	
8	**Characterization**			
8.1	Characterization	SEM 2 or 3	Cleave test wafer and look at the trench in the SEM. We should be able to see an Au seed layer at the bottom of the trench.	
9	**Electroplating**			
9.1	Gold electroplating	Use electroplating setup or beaker	**Plating parameters:** Current density: 10mA/cm2 Pulse ratio: 1:5 Ratio ON-OFF: 4ms:20ms Cycle length: 24ms **Electrolyte:** Gold cyanide Concentration: 15 g/L	This step was performed in a fumehood at DTU Mechnical Engineering due to the restricion of cyanide use at DTU Nanolab. Contact Peter Westerman at DTU Mechanic. **NOTE**: lower concentration of gold induces plating issue (i.e. side wall deposition, voids)