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Precise Timing Control in Deep Reactive Ion Etching (DRIE) with Bosch Process

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January 18, 2017

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1 Introduction

As use of electrical and optical components grow larger so does the demand of the production. In the last decades the development has made components smaller and smaller as Moore's law proves its worth. In order to continue this development, techniques and machinery that can create structures in nanoscale is required. DTU Danchip works from a principle that it would rather predict the procedures that will be needed in the future and optimize them so that they are ready for use when the time comes than they will develop the procedure when it is already needed. Other scientists have managed to develop 200 nm silicon gratings with an aspect ratio of around 60 (Mukherjee et al., 2010) and below 40 nm dimater silicon pillars with an aspect ratio greater than 50 (Morton et al., 2008).
This report is concerned with optimizing the Bosch process, a form of Deep Reactive Ion Etching (DRIE), on DTU-Danchips DRIE-Pegasus machine. The optimization in this report is mainly concerned with two main areas:

- Measuring time errors and reduce its influence for a precise timing control of the process.
- Development of recipes for etching trenches with the DRIE-Pegasus.

In doing so, the hope is that, in time, it will be possible to develop a systematical procedure to achieve high aspect ratio etching with a good profile that can be used for among other things optical purposes.

2 DUV Exposure

The pattern on the 6" silicon wafer used for the DRIE process (see section 3) was made using DUV exposure. First, a Bottom Anti-Reflective Coating layer, abbreviated BARC layer, was deposited on the wafer using spin coating. The wafer was spun at 4700 rpm for 30 seconds and then baked at 175° Celsius for 90 seconds. The expected thickness was 65nm. This layer prevents standing waves and reflections damaging the pattern during the DUV exposure.
Next a layer of positive photo resist was applied by spinning for 30 seconds at 2500 rpm and baking it for 90 seconds at 130 ° Celsius. The expected thickness of the resist layer was 360 nm. The Positive resist has the characteristic that it gets soluble when exposed to DUV light. The DUV stepper in DTU Danchip was used to apply a reticle to the wafer and exposing the resist not covered by the reticle to DUV light. Three wafers were made using three different reticles:

- 5 µm trenches with 50 µm pitches.
- 1 µm trenches with 10 µm pitches.
- 0.2 µm trenches with 2 µm pitches.

After the DUV stepper the wafers were baked for 60 seconds at 130 ° Celsius and developed for 60 seconds in AZ MIF 726 (2.38% TMAH). The development is the process that removes the soluble photoresist, thus creating the patterns.
The result of this process was three wafers with 16 7 × 7 mm chips. These wafers were afterwards *cleaved* in order to separate the 16 chips. Each of these chips could then be placed on a*carrier wafer* coated by aluminium which was then inserted into the DRIE Pegasus in order to make several tests using only the one wafer with a pattern engraved.

2.1 SEM image and dataanalysis

After the DUV exposure process the three samples were examined in a Scanning Electron Microscope (SEM). The line width and uniformity of the wafers was examined by taking a top view picture and the shape of the trench was found using a cross-section image. This step is crucial because an acceptable uniformity of patterns is the basis for analysis of etch results. Figures 1,2 and 3 show a top view of the three different patterns without any measurements.

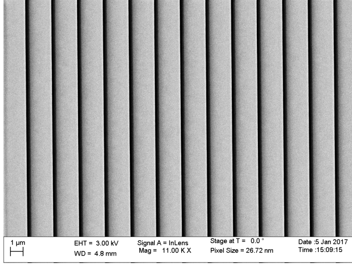

Figure 1: Top overview of the 0.2 µm trench wafer

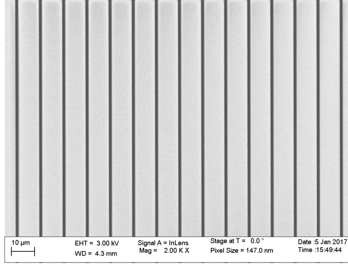

Figure 2: Top overview of the 1 µm trench wafer

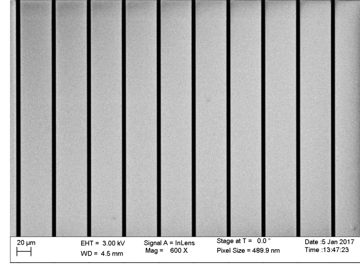

Figure 3: Top overview of the 5 µm trench wafer

After observing the patterns were indeed trenches as desired the line width of each wafer was measured by zooming in so that only 4 lines could be observed. This is illustrated in figures 4, 5 and 6. The actual measurements cannot be read from the picture but is listed in table 1.

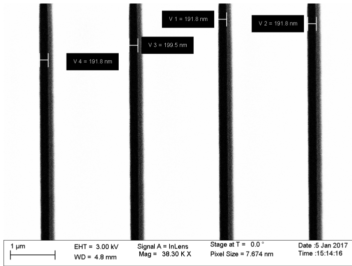

Figure 4: Zoom in of the 0.2 µm wafer showing measurements of line width. See table 1 for actual data.

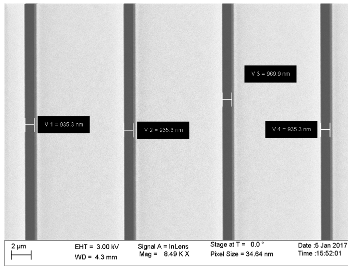

Figure 5: Zoom in of the 1 µm wafer showing measurements of line width. See table 1 for actual data.

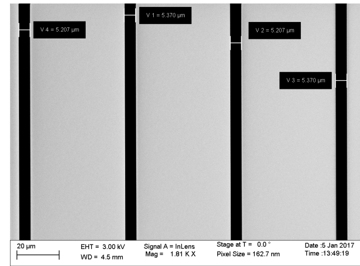

Figure 6: Zoom in of the 5 µm wafer showing measurements of line width. See table 1 for actual data.

We measured a single pattern 4 different places and five different patterns. These measurements are used to find the uniformity of both the individual pattern and the entire wafer. Uniformity is defined as:

$$U := \frac{\max - \min}{2 \cdot \text{average}} \tag{2.1}$$

For this wafer the uniformity across the wafer thus becomes

$$U = \frac{0.992 - 0.946}{2 \cdot 0.973} = 0.024 = 2.4\% \tag{2.2}$$

This as well as the uniformity of a single pattern was calculated for both the 1µm and the 5µm wafer along with the standard deviation. In out case, a uniformity below 5% is accepted.

	Center chip	Left chip	Right chip	Top chip	Bottom chip
Measurement 1 [μm]	0.921	1.010	0.978	0.983	0.973
Measurement 2 [μm]	0.920	0.975	0.978	0.983	0.973
Measurement 3 [μm]	0.990	0.975	0.978	0.983	0.937
Measurement 4 [μm]	0.955	0.975	0.943	1.019	1.009
Average [μm]	0.946	0.984	0.969	0.992	0.973

Table 1: Measurements as well as the calculated average of five different patterns placed different places on the 1 μm wafer. All measurements are in μm

	1 μm wafer	5 μm wafer
Average pattern linewidth [μm]	0.949	5.494
Pattern linewidth SD [μm]	0.018	0.162
Pattern uniformity [%]	2.27	3.00
Average wafer linewidth [μm]	0.973	5.501
Wafer linewidth SD [μm]	0.017	0.0182
Wafer uniformity [%]	2.36	4.25

Table 2: The average linewidth of the 5 μm and 1 μm wafer with calculated standard deviation and uniformity for both an individual pattern and the entire wafer.

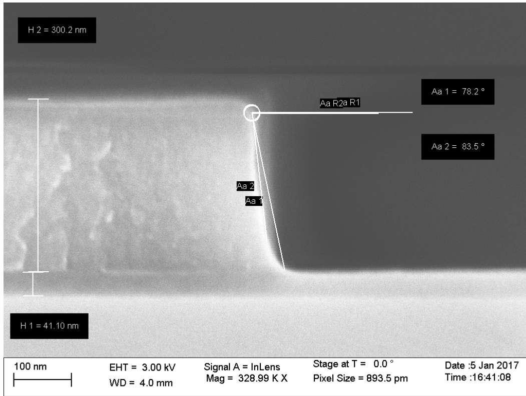

Figure 7: SEM crosssection of the 1 μm wafer showing the actual thickness of the BARC layer and the photoresist.

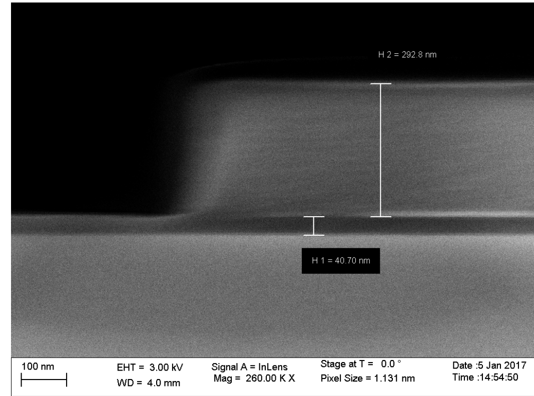

Figure 8: SEM crosssection of the 5 μm wafer showing the actual thickness of the BARC layer and the photoresist.

Afterwards, the chip was cleaved again and a cross section of the 1 μm and 5μm wafer was examined using the SEM. This is shown in figures 7 and 8.

The measured thicknesses was around 41 nm of BARC which was expected to be 65 nm and around 300nm photoresist which was expected to be 360nm. The uniformity and crosssection examination was only done for the 1 μm and the 5 μm wafer since the uniformity of the 0.2 μm wafer was very poor. The DUV exposure dose did not give the sought result for the 0.2 μm wafer as can be seen in figure 9. Some of the lines are smaller than 200 nm which might be due to an underexposure or error during the DUV stepper's calibration. This led to a *dose test*.

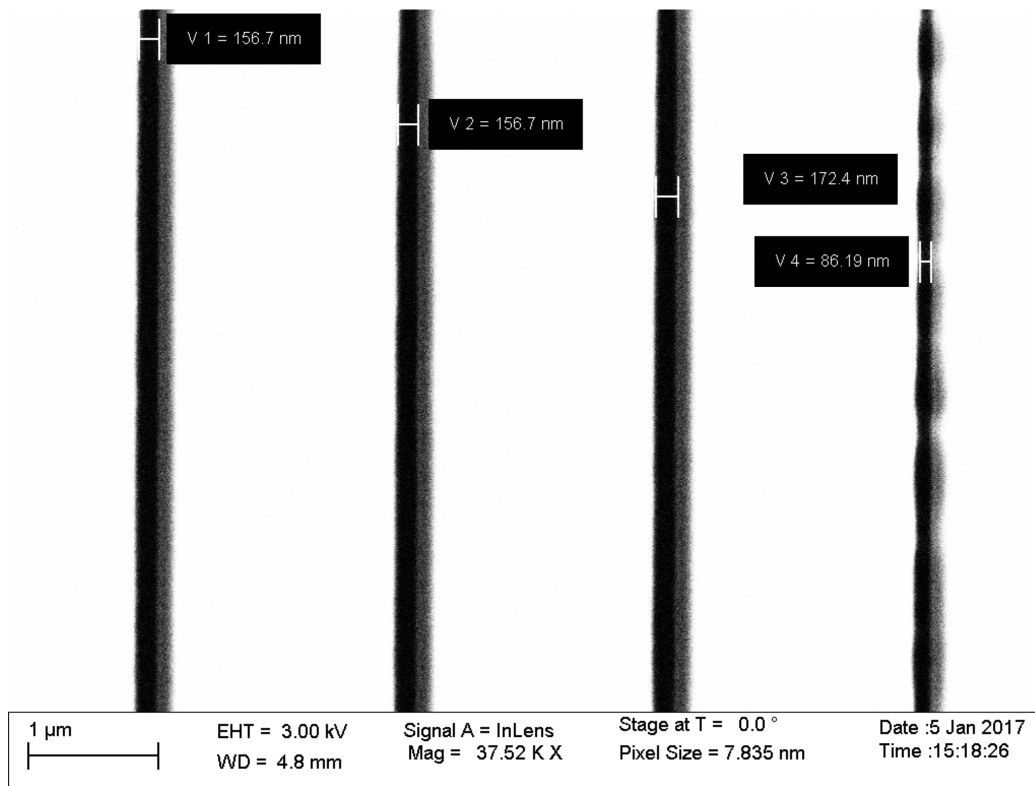

Figure 9: SEM picture of the first 200 nm water. The linewidths differ greatly and the wafer was therefore discarded.

2.2 Dosetest for 200 nm pattern

A dose test is a process where a wafer is exposed to, in our case, 16 different DUV intensities and the resulting pattern is examined in a SEM to see at which dose the pattern has the desired linewidth and thickness. The first 200 nm wafer was made using 280 $\frac{\mathrm{J}}{\mathrm{cm}^2}$ so the test was made with doses ranging from 260 $\frac{\mathrm{J}}{\mathrm{cm}^2}$ to 410 $\frac{\mathrm{J}}{\mathrm{cm}^2}$ by increments of 10 $\frac{\mathrm{J}}{\mathrm{cm}^2}$.

The result, shown in figure 10, yielded a desired dose intensity of approximately 350 $\frac{\mathrm{J}}{\mathrm{cm}^2}$ as opposed to the 280 $\frac{\mathrm{J}}{\mathrm{cm}^2}$ suggested by Danchip staff. In the graph some of the data points have been omitted for simplicity. As a dosetest has been made earlier where the optimal dose was 280 $\frac{\mathrm{J}}{\mathrm{cm}^2}$ this pointed to an error concerned with the DUV stepper and the 200 nm wafer was therefore dropped.

3 Deep Reactive Ion Etching

In general, there are many different etching techniques. Each of them have varying pros and cons and are thus used for different purposes. One of the most popular techniques when etching deep in a material with a high aspect ratio is called a Deep Reactive Ion Etching process. This process etches the material using both chemicals and ions as the name implies. The setup is shown in figure 11 (Veiko Lindroos, 2009). The gas is led through the gas inlet and through the inductive coil where the gas is excited, and a fraction of it ionized, before it enters the chamber. The wafer is placed upon the platen, an AC source with the same frequency as the coil that has

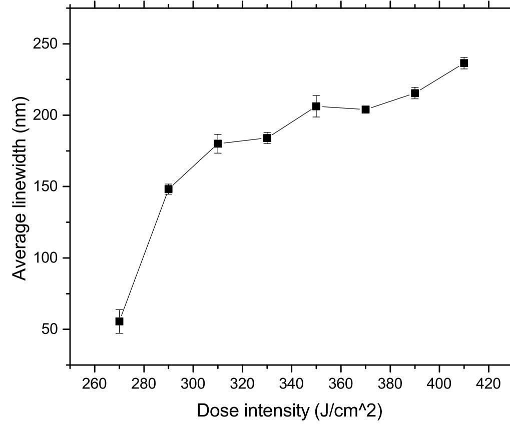

Figure 10: Average linewidth for different dose intensities. The desired intensity is around 350 $\frac{\mathrm{J}}{\mathrm{cm}^2}$ as opposed to the 280 $\frac{\mathrm{J}}{\mathrm{cm}^2}$ used originally.

been negatively biased by a DC source. This negative bias ensures that the platen is always less positive than the inductive coil and attracts the ions to the wafer. The machine we are using is the DRIE Pegasus (SPTS).

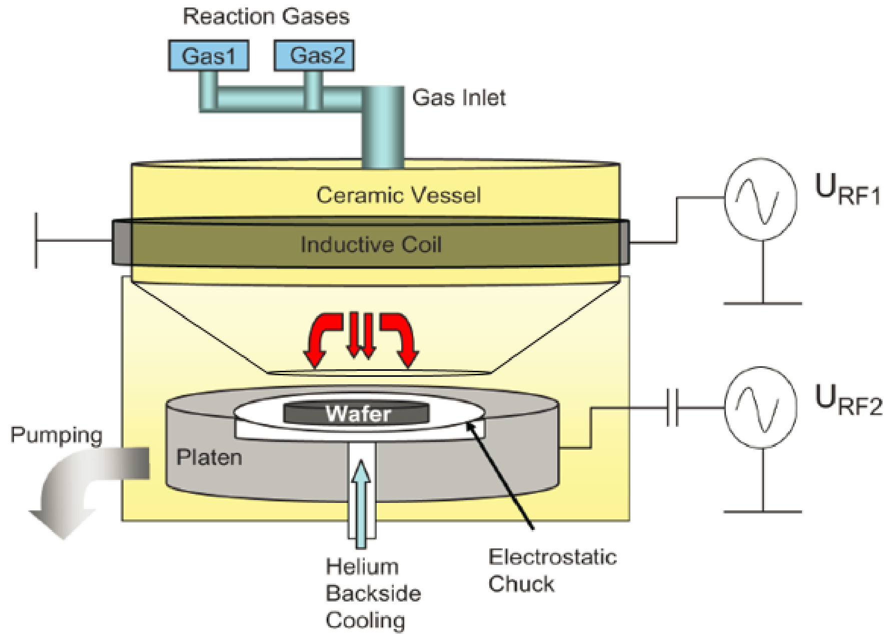

Figure 11: A sketch of the DRIE chamber. Modified from (Veiko Lindroos, 2009)

3.1 Bosch Processes

The Bosch-procces is a DRIE-etching process that alternates between isotropic etching and deposition of a passivation layer to achieve deep etching with high aspect ratio and relatively low sidewall roughness.

For each passivation cycle a Teflon®-like film, formed from C_4F_8, is applied to the whole trench protecting it from etching. During the etching cycle the passivation layer at the bottom of the trench is removed by the (near) vertical ion bombardment and etching occurs. The etching chemical used in a Bosh-process is SF_6 which lead to an isotropical etching at the exposed areas (Veiko Lindroos, 2009).

3.2 Two-step Bosch process

The two-step Bosch process is what is usually understood to be the Bosch process. It is a two cycle process consisting of the previously explained steps of etching and passivation. This process creates *scallops* as a result of the chemical etching. The scallops are the half-circles that occur on both sides of the channel when etching this way. They can be seen in figure 12 or clearer in figure 24. Optimally, the process should create approximately straight walls by minimizing the size of the scallops. The process is shown in figure 12

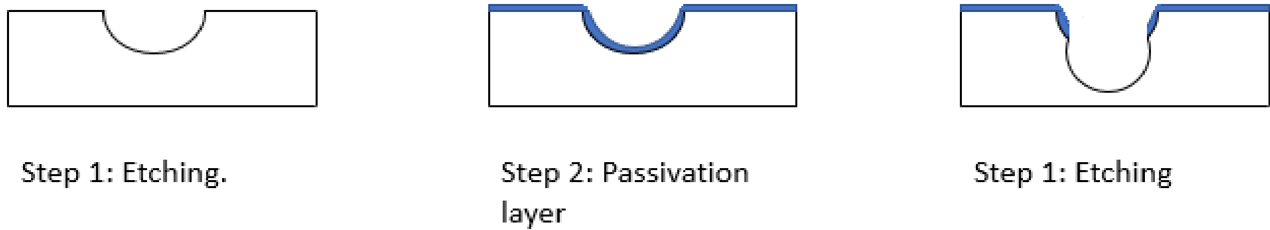

Figure 12: A sketch of the two-step Bosch process.

3.3 Three-step Bosch process

The three-step Bosch process is a proposed improvement to the regular two-step Bosch process.

It is proposed that the aspect ratio and sidewall roughness can be improved by adding a third phase of *boost etching* in the etching cycle to take place after the deposition of the passivation layer. This is a short cycle of low SF_6 concentration in the chamber combined with a high negative potential at the platen, which gives a vertical and high energy ion-bombardment. The process is sketched in figure 13

The intention is to quickly break the passivation layer at the bottom of the trench so that the following cycle of etching can take place with no DC-bias at the platen. This gives two main advantages:

- It will allow for a higher selectivity between Si and the passivation layer and mask, since less ions will be present during the main etching cycle.
- It can lead to less sidewall scalloping, due to the possibility of slower etch rates.

3.4 Timing issues

Several timing issues has been discovered while working with the DRIE-Pegasus. In the following their existence will be shown and suggestions will be given on how to best counteract them. As an overview of the issues discussed we refer to figure 14.

While it is outside the scope of this report to determine the reason for these time fluctuations in the DRIE-Pegasus we will present the current hypothesis by Professor Henri Jansen (DTU-Danchip) to give our readers a sense of what is likely causing the issues. This also gives an insight into how we came about the solutions that will be suggested in the remainder of this section.

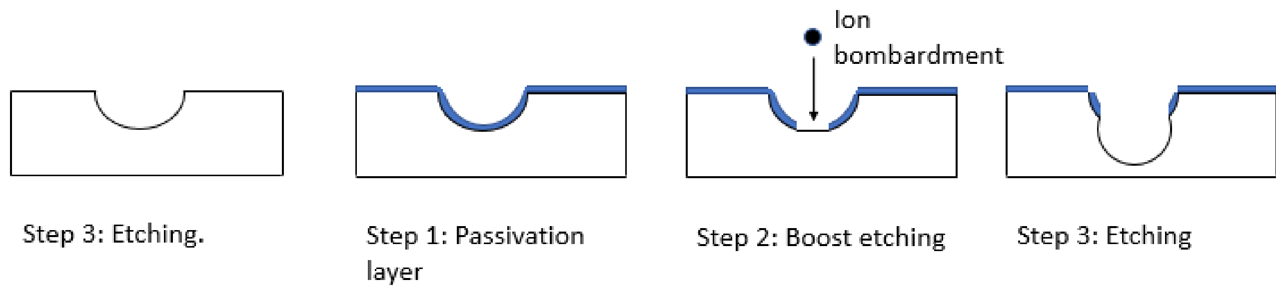

Figure 13: A sketch of the three-step Bosch process.

Professor Jansen is currently working with the hypothesis, that time fluctuations are caused by cycle time in the Programmable Logic Controller (PLC) responsible for shifting all sub processes on and off. By his estimations the PLC has a 70 ms cycle time to run through all sub-processes.

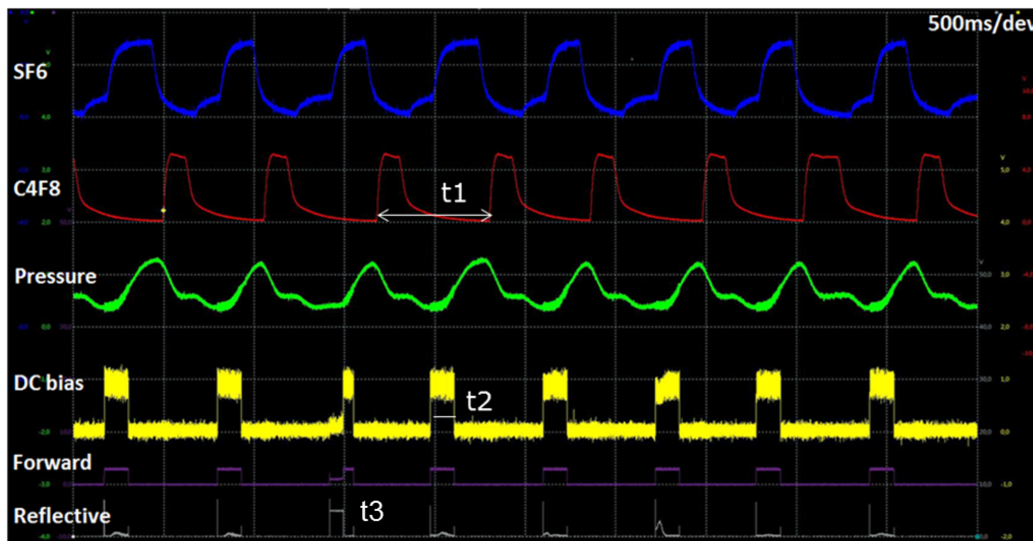

Figure 14: A screenshot from the Picoscope showing the significance of the different channels and the three timing issues discussed. Forward and reflective refers to forward- and reflective power.
On the figure can be seen the effect of all three timing issues. t1 is the total cycle time, t2 is the boost time and t3 shows the effect of having a matching unit set wrong.

3.4.1 Fluctuation of total cycle time

Users of the DRIE-Pegasus have been reporting inconsistencies in the total cycle time when running with short switching times and thus short total cycle times. The total cycle time is represented on figure 14 as t1.

To prove there is a problem with the total cycle time we have constructed a simple experiment. A series of Bosch-processes where run with the DRIE-Pegasus set for a specific total cycle time and the actual total cycle time recorded with a PicoScope (digital oscilloscope by Pico Technologies). This was done for a series of different switching cycles of varying time. We then calculated the average period for the given switching time and the standard deviation. The resulting standard deviations are seen on figure 15 with respect to the programmed total cycle time.

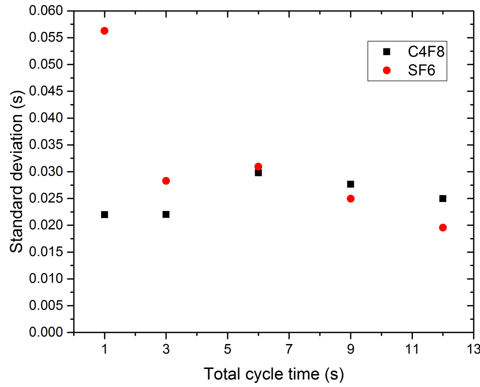

Figure 15: Standard deviation on the total cycle time with respect to the programmed switching time. We suspect that the datapoint for SF6 at 1s is an error of measurement.

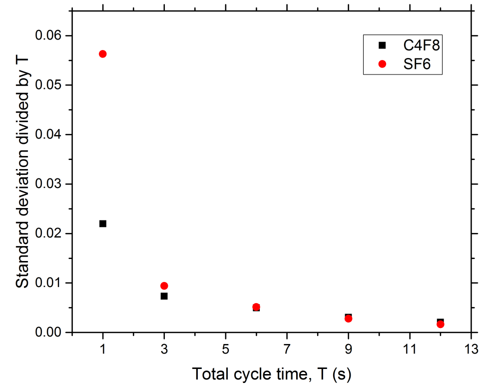

Figure 16: Standard deviation divided by the total cycle time with respect to the programmed total cycle time. We suspect that the datapoint for SF6 at 1s is an error of measurement.

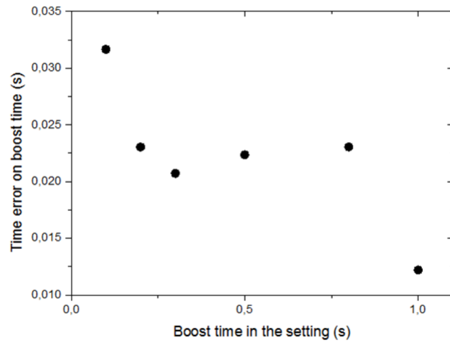

Figure 17: Time error on boost time. See figure 19 for a graph of the used data.

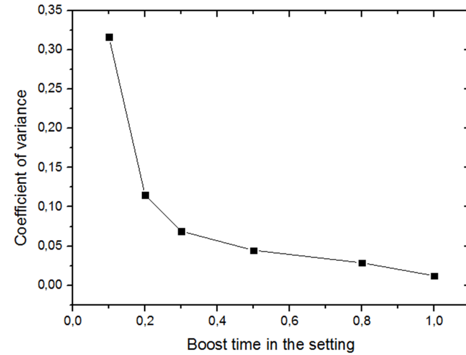

Figure 18: Coefficient of variance for the boost time fluctuation. See figure 19 for a graph of the used data.

It is seen from figure 15 that the standard deviation is approximately constant over different switching times. Thus there is a constant time error on the DRIE-Pegasus which appear to be independent of total cycle time.

A way to overcome the effect of the fluctuation is to increase the cycle time. By doing this, the relative impact of the error becomes less and therefor we anticipate that it should be possible to get consistent results from cycle to cycle. This principle is shown in figure 16, where we have calculated the standard deviation divided by the total cycle time for several different total cycle times.

3.4.2 Fluctuation of boosttime on platen power

Another time fluctuation was discovered on the DC-bias of the platen while boost etching, see t2 on figure 14. A statistical approach can be seen in figures 17, 18 and 19 where the large variations deviate by over 0.5 s from the average and thus gives a significant variation for small boost times. The effect on the etching process is, that a nonuniform amount of ions is directed to the silicium, leading to a non-uniform removal of the passivation layer in the trench.

From figure 19 it is also seen, that for the low switching time the DRIE-Pegasus is unable to deliver the selected boost-time, which makes recipes harder to develop, since the chosen setting might not give the desired boost-time.

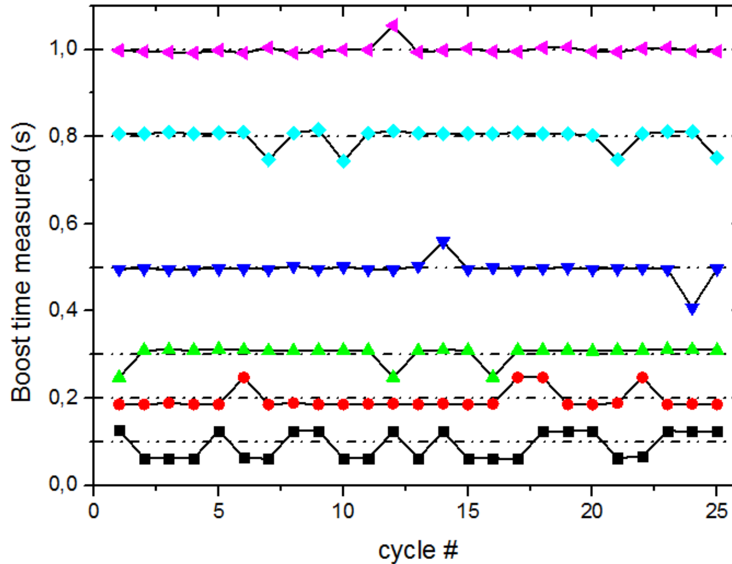

Figure 19: Boost time of the DC-bias on the platen. The dotted line represents the selected boosttime while the datapoints represents the boostime as measured by the Picoscope.
All credit for this graph goes to our supervisor, Bingdong Chang, from who we borrowed this.

As in Section 3.4.1 one way to negate the relative effect of the time fluctuation is to increase the boost time. While this is possible it has undesired side effects: If the DC-bias is kept constant and the time increased more ions will hit the wafer per cycle. This will cause a quicker depletion of the photo-resist and therefore limit the dept of the trenches. If the DC-bias is lowered and the time increased the ions will have less energy and will more easily be deflected away from vertical by collision with gas particles. This could lead to undercutting.

Another way to solve the problem was developed by Professor Jansen. He designed an external timing unit, named *Pega Pulser*, which bypass the PLC. When active the Pega Pulser is in direct control of the amplitude and duration of the DC-bias on the platen. Using this solution lead to precision on the scale of a few milliseconds. The Pega Pulser thus negate the boost time fluctuation while maintaining the possibility of short boost-times.

3.4.3 Fluctuation of the matching unit

The conditions inside the DRIE-Pegasus when the plasma is on can be viewed as an electrical circuit. Generators feed power to the upper coil which is connected to the platen through the electrically conducting plasma. Because the plasma conditions can vary depending on how it is used the DRIE-Pegasus has a matching unit capable of adjusting the impedance of the circuit. The desire is to tune the matching units into the optimum positions where power is transferred to the load with as little power reflected back to the generator as possible. An example the effect if the matching unit is not placed correctly can be seen on figure 14 as t3.

Normally the matching unit is automatically controlled by the Pegasus, but users have been reporting fluctuation during the etching as can be seen in figure 20. It seems that the even though the machine is set at approximately optimal placement from the beginning it will vary the matching unit in an attempt to find a better placement. This causes it to fluctuate before returning to the initial position. Since the path taken to re-reach the optimum varies from etch to etch it is not possible to guarantee a consistent result.

The simplest solution which allowed for a repeatable result was to manually take control of the matching unit and set it to a precalibrated value. This gave additional, but acceptable, problems: Firstly it necessitated 10-15 minutes preconditioning of the machine before the parameters reached equilibrium and we could load the wafer. Secondly it resulted in slightly more reflected power. This was deemed an acceptable sacrifice, since it was consistent from etch to etch. Thirdly it posses a risk to the health of the Pegasus. If the reflected power reaches a critical level the power generators will be damaged. It thus requires solid recipes or attentive users to function.

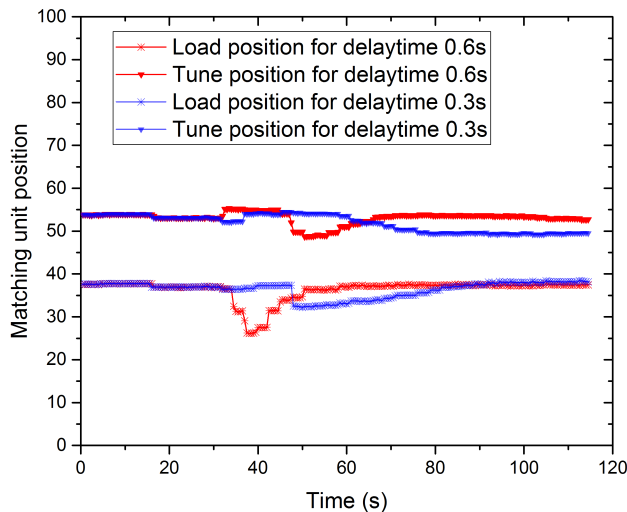

Figure 20: Variation of the matching unit when in automatic mode. On the figure is shown two different examples of the automatic variation, which differs by their delaytime after which the boost phase takes place. While the matching unit is separated into *Load* and *Tune* we do not differ in the report, since they both change the impedance.
The units on the second axis is percentage of the total matching capability and is thus a rather arbitrary unit.

4 Recipe development

'Correcting' the timing errors led to actual etching of the different patterns. We started out with the recipe "PP fast 3.1", a previous recipe by Professor Jansen. To control the process we fixed all paramters, but C_4F_8- and SF_6 gasflow and the platen power boost time.

4.1 PP fast 3.1

The first etching was made on a 5 µm pattern and a 1 µm patterm using a 4" aluminium wafer as carrier wafer. The C_4F_8 flow was 100 sccm, the SF_6 flow was 300 sccm during the boost period and 600 sccm during the main period. The platen power time was 0.133 seconds. For simplicity the remainder of the paramaters can be seen in the Appendix. The results of the given parameters are shown in figure 22 and 21.

The aspect ratio was around 5 and 15 for the 5µm wafer and the 1 µm wafer respectively, but both had other problems. The 5 µm wafer still had some grass (silicon residue) in the bottom of the trench and both wafers became narrower when etching deeper into the material. To avoid the narrowing of the etch, *ramping* was introduced. Ramping is a process where the etching gas concentration is increased with time so that there is a

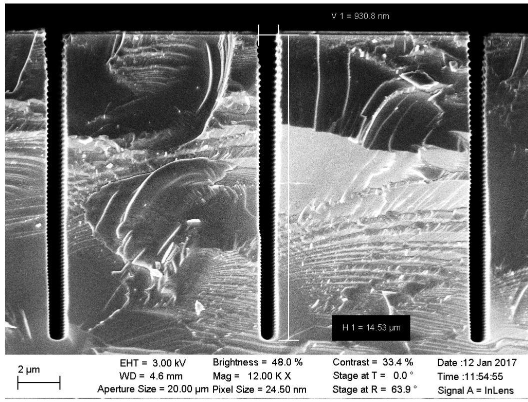

Figure 21: SEM cross section of the 1 µm wafer showing the selectivity of the etch. It can be seen that the etch is not entirely straight.

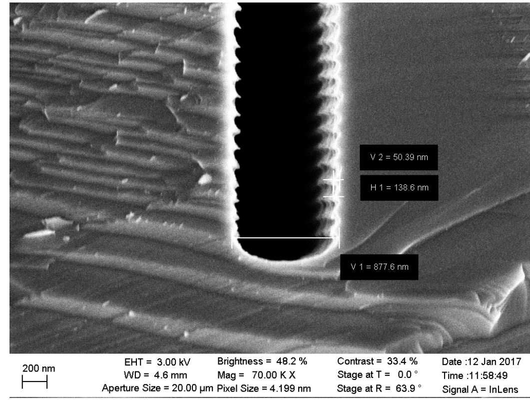

Figure 22: SEM cross section of the 1 µm wafer showing the bttom of the trench.

higher gas concentration in the end than in the beginning. This makes the scallops and the etching rate more uniform since less and less gas will reach the bottom of the etch as the etch grows deeper if the concentration is unchanged. This is also known as *RIE-lag* (Franssila, 2010).

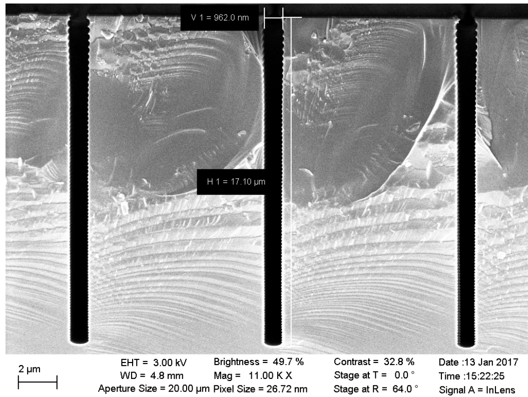

Figure 23: SEM cross section of the 1 µm wafer etched with ramping and a 200 ms platen power time. The selectivity is now around 18, the etch is straight, the scallops are uniform and the grass is gone.

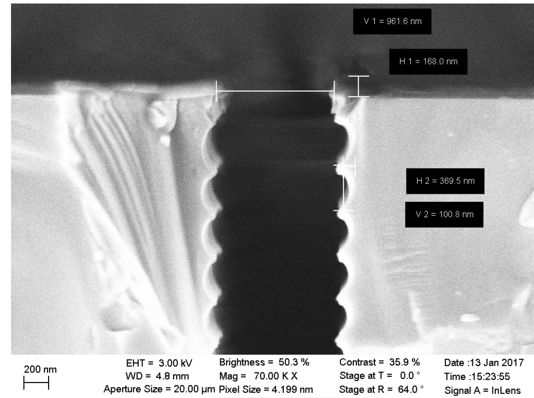

Figure 24: SEM cross section of the top of the 1 µm wafer. The photoresist and BARC layer has a total depth of around 160 nm.

4.2 PP fast 3.2

In order to remove the grass and straighten the sidewalls, the platen power time was increased from 133 ms to 200 ms and ramping was employed linearly ramping the SF_6-flow from 300 sccm to 1200 sccm during the etch. C_4F_8 was kept constant from 3.1 to 3.2.
Changing these parameters gave a straighter, deeper etch with an aspect ratio of around 18, which can be seen in figures 23 and 24. The photoresist was also etched for a longer time which resulted in a very thin remaining photoresist layer. Since etching any longer with these settings would likely etch through the photoresist this

prevented a new etch with a very long etching time to see if the etching profile would remain straight and with uniform scallops. Some parameters were therefore changed.

4.3 PP fast 3.3

The platen power time was reduced from 200ms to 150ms to reduce the etching of the photoresist and the ramping was changed to go from 50 sccm to 1200 sccm to get smaller scallops in the top of the trench. This resulted in a quite straight etching with an aspect ratio of around 27 which can be seen in figure 25. Figure 26, however, shows that there is almost no resist left on top of the silicon. In fact there is only around 17 nm of BARC left.

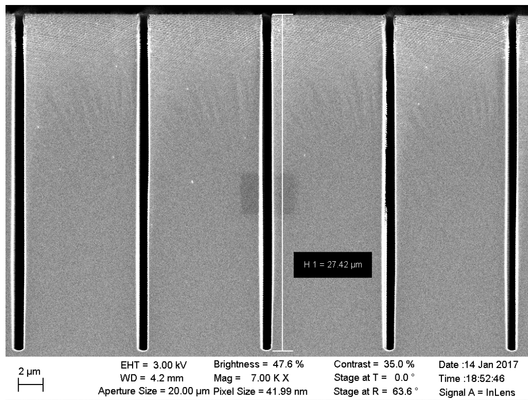

Figure 25: SEM cross section of the 1 µm wafer etched with ramping from 50 sccm to 1200 sccm and a 150 ms platen power time. The selectivity is now around 27, the etch is straight, the scallops are uniform and the grass is gone.

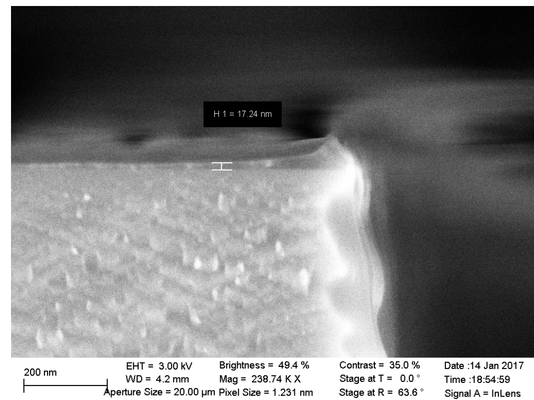

Figure 26: SEM cross section of the top of the 1 µm wafer. The photoresist is gone and there is approximately 17nm BARC left.

The aluminium carrier wafer used for all the samples was, however, barely etched. The next step could therefore be to create a hard mask made of aluminum, thus allowing for a longer etch time.

5 Conclusion

Three 6" wafers with trenches with a linewidth 5 µm, 1µm and 200 nm respectively was made using spin coating and DUV exposure. The 200nm wafer was discarded due to the process creating a non-uniform pattern. The other two wafers were cleaved and attached to an aluminum carrier wafer which was inserted into the DRIE pegasus.
Several timing issues with DTU-Danchip's DRIE-Pegasus has been proven. It was found that it has a fluctuation of the total cycle time, a fluctuation of the DC-bias on the platen and an inability to maintain the matching unit at a steady position.

These were corrected by having a long total cycle time, installation of the *Pega Pulser* and by assuming manual control of the matching unit.

Having corrected the timing issues we went on to recipe development. We showed that with these corrections in place it was possible to make straight trenches of acceptable aspect ratio. An aspect ratio of 27 was achieved this way but one shortcoming proved to be the selectivity of the photoresist which limited the etching time. Therefore a hard mask made of aluminium was proposed.

We have no results based on the aluminium mask but believe it will achieve higher aspect ratio since the thickness of the photoresist will no longer be an issue. When the photoresist and BARC layer has been etched away, there will still be an aluminium mask remaining which is not etched in the process.

6 Appendix

<table>
<tr><td colspan="8">1</td></tr>
<tr><td colspan="8">Purpose: presetting load and tune positions to be 1 and 1, a dummy wafer was run first to stabilize the reflective power signal,</td></tr>
<tr><td colspan="8">Recipe: PP fast 3.1 (folder of bincha)</td></tr>
<tr><td colspan="8">Substrate: chips with 5µm lines by DUV resist, 4” Si wafer with around 200nm ALD grown alumina as carrier wafer.</td></tr>
<tr><td colspan="8">Parameter settings</td></tr>
<tr><td colspan="2"></td><td colspan="3">Deposition</td><td colspan="3">Etch</td></tr>
<tr><td colspan="2"></td><td>Delay</td><td>Boost</td><td>Main</td><td>Delay</td><td>Boost</td><td>main</td></tr>
<tr><td colspan="2">C4F8</td><td>0/0</td><td>0/0</td><td>1.0/100</td><td>0/0</td><td>0/0</td><td>0/0</td></tr>
<tr><td colspan="2">SF6</td><td>0/0</td><td>0/0</td><td>0/0</td><td>0/0</td><td>0.1/300</td><td>1.6 /600</td></tr>
<tr><td colspan="2">Throttle</td><td>0/0</td><td>0/0</td><td>1.0 /100</td><td>0/100</td><td>0.1/100</td><td>1.6 /100</td></tr>
<tr><td colspan="2">Platen</td><td>0/0</td><td>0/0</td><td>1.0 /1</td><td>0.6/1</td><td>PegaPulser controlled
Amplitude: (9,0)
Time: 133ms</td><td>1.6 /1</td></tr>
<tr><td colspan="2">ICP</td><td>0/0</td><td>0/0</td><td>1.0 /4999</td><td>0/0</td><td>0/0</td><td>1.6 /4999</td></tr>
<tr><td rowspan="2">Coil (A)</td><td>L</td><td colspan="3">30</td><td colspan="3">30</td></tr>
<tr><td>T</td><td colspan="3">55</td><td colspan="3">55</td></tr>
<tr><td rowspan="2">Platen (M)</td><td>L</td><td colspan="3">35.5 (initial 1 for 0.2s)</td><td colspan="3">35.5 (initial 1 for 0.2s)</td></tr>
<tr><td>T</td><td colspan="3">52.7 (initial 1 for 0.2s)</td><td colspan="3">52.7 (initial 1 for 0.2s)</td></tr>
<tr><td colspan="2">Other</td><td colspan="6">Temperature -19C;
S=E, E=E,
Total cycles 100, total etch time 4min20s.</td></tr>
</table>

Figure 27: A datalog by Bingdong Chang showing the Pegasus paramaters for PP Fast 3.1

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