Technical University of Denmark

33470 Mikro 3W
(3 weeks course)

High Resolution Pattern Definition with E-beam Lithography

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1 Introduction

1.1 Motivation

The goal of this project is to optimize the precision and resolution of nanoscale structures, mainly lines, made with Electron Beam Lithography (EBL), which is an important technique for defining high resolution patterns for etching or molding purposes. HSQ (hydrogen silsesquixane) has a very high resolution making it the perfect resist for this task. Already sub 10 nm[1] and sub 5 nm[2] structures have been obtained. Several uses for these small structures have been found e.g. Hard discs structures with bit-patterned media beyond 1.5 Tbit/inch^2[3] and single-electron transistors[4]. Also it can be used directly as an etching mask, because of the high selectivity with regards to silicon. To reduce the critical dimension of the structures, the optimal soft baking temperature, developing temperature and developing time will be found using a factorial design analysis. Appropriate parameters will be found for spin coating the thinnest resist possible to reduce forward and backward scattering, and the exposure dose will also be optimized.

1.2 Process flow

A brief summary of the process flow, describing the different steps of the experiment can be seen below. For entire description see appendix 1. All processes have been carried out in DTU Danchip's cleanroom.

- Spin coating sub 100 nm HSQ resist on silicon wafers, thickness characterization with ellipsometer.
- Soft baking of coated wafer at 80 °C in various time.
- Electron Beam exposure with various doses from 20 000 - 42 000 µC/cm^2.
- Developing with various temperatures from 22-35 °C using sodium hydroxide (NaOH) as developer.
- Characterizations of structures with SEM (Scanning Electron Microscope).
- Pattern transfer with ASE (Advanced Silicon Etcher).

1.3 Monte Carlo Simulations

A Monte Carlo simulation of the electron dispersion within the material was done by using TRACER (GenlSys GmbH). This was done to show, what happens when you have a thinner resist thickness. From the simulations in figure 1, it is seen that forward scattered electrons travels deeper into the resist and substrate. Thus a broader area of resist will be exposed and cross linked. Therefore a thinner resist is desirable to reduce the forward scattering.

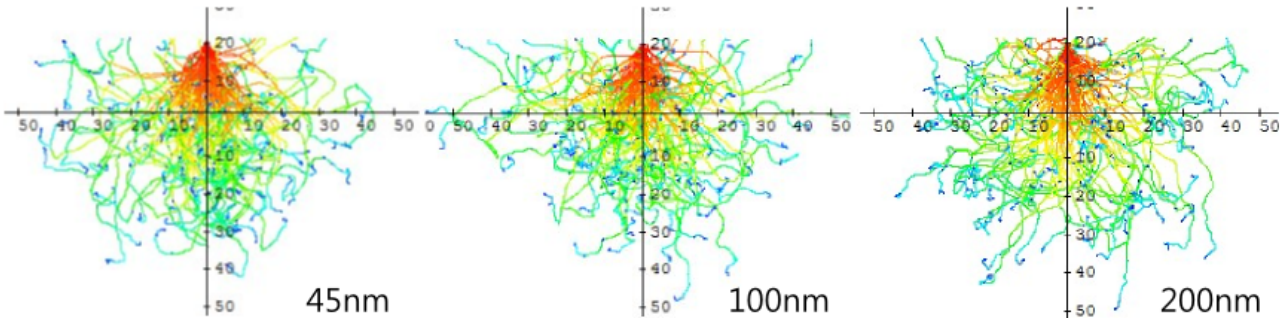


Figure 1: Monte Carlo Simulation of forward scattered and back scattered electrons with 100 electrons and an acceleration voltage of 100 keV. HSQ is used as resist with various thicknesses of 45, 100 and 200 nm respectively and a silicon substrate with a thickness of 500 µm. The highest energy electrons are red and the lowest energy electrons are blue. The simulations are made in TRACER, (GenlSys GmbH).

HSQ thickness	α	β	η	ν_1	ν_2	γ_1	γ_2
200 nm	0.001155 μm	31.971589 μm	0.365318	0.365318	0.046466	33.0399 μm	0.0101 μm
100 nm	0.001018 μm	27.569093 μm	0.244937	0	0	27.5691 μm	27.5691 μm
45 nm	0.0010 μm	32.0221 μm	0.2277	0.2185	0	32.1365 μm	32.1365 μm

Table 1: α, β, η, ν_1, ν_2, γ_1, γ_2 and r are parameters for a multi Gaussian function. In this case a Point Spread Function with 100 electrons and an acceleration voltage of 100 keV, for HSQ resist thickness of 200 nm, 100 nm and 45 nm, respectively. The simulations are made in TRACER, (GenlSys GmbH).

From the parameters in table 1, a Point Spread Function (PSF), can be calculated:

$$PSF(r) = \frac{1}{1+\eta+\nu_1+\nu_2}\left(\frac{1}{\pi\alpha^2}e^{-\frac{r^2}{\alpha^2}} + \frac{\eta}{\pi\beta^2}e^{-\frac{r^2}{\beta^2}} + \frac{\nu_1}{\pi\gamma_1^2}e^{-\frac{r^2}{\gamma_1^2}} + \frac{\nu_2}{\pi\gamma_2^2}e^{-\frac{r^2}{\gamma_2^2}}\right) \quad (1)$$

Looking at the PSF on figure 2 it is seen that the first bump on the graph is the amount of forward scattered electrons and the second bump is the backscattered electrons. Though it seems like there isn't any backscattering for the thinner resist, there certainly is, the deviation is just so small that it doesn't show up on the double log plot.

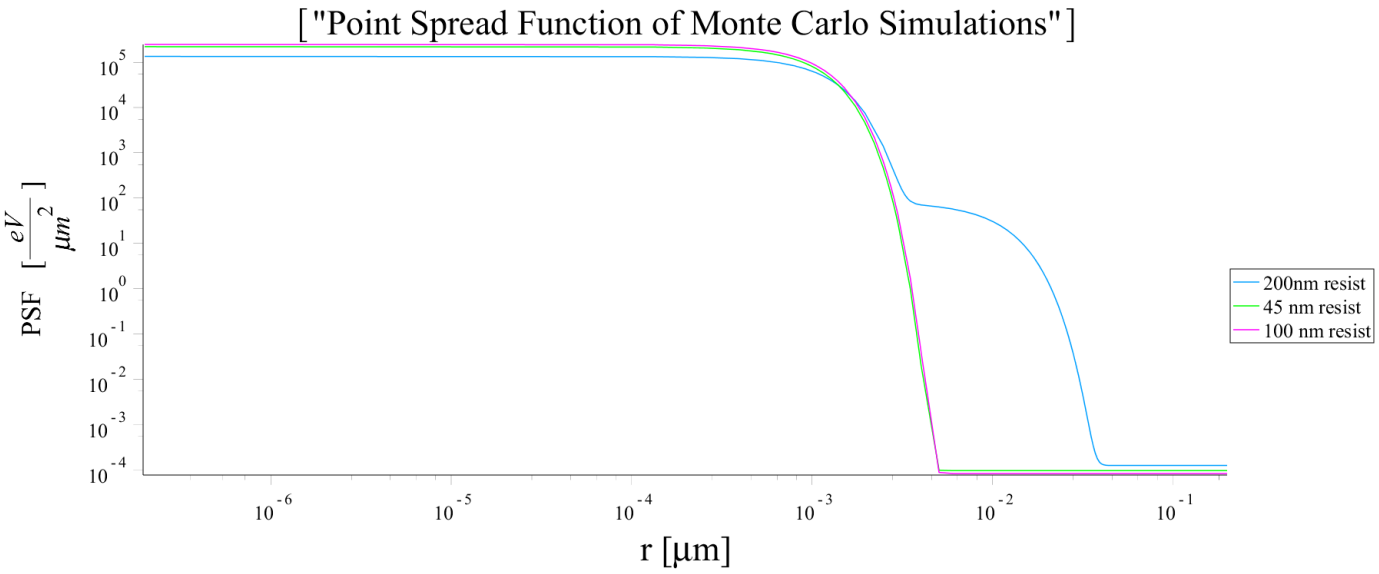


Figure 2: Point of Spread Function double log plot for 45, 100 and 200 nm thick HSQ resist, calculated from the multi gaussian function parameters in table 1.

Figure 2 tells us that the thicker resist has a lot more back scattered electrons than the thinner resist. And this is what makes a thinner resist desirable for defining small features, to limit the backscattering and thereby reducing the proximity error for dense lines.

2 Experimental Methods and Results

To optimize the final structures it is needed to optimize the individual steps in the process flow. In this section the different steps are described, results of the initial measurements are presented and finally a factorial experiment design method is used to optimize the parameters.

2.1 Spin coating

2.1.1 Spincurves

The masking material used in this set-up is HSQ with a concentration of 2% and 6%. HSQ is chosen because of its high resolution and that it can be spin coated in quite small layers, due to its small molecules. The

wafers were manually spin coated by using a manual spin coater for standard resist. The patterns are to be defined with EBL, therefore to minimize the impact of the proximity effect of the resolution of a pattern, several countermeasures must be taken. One of these is to reduce the thickness of the mask, since the electrons will have less medium to propagate in before potentially being stopped by the material.
Several parameters can be changed to obtain a thin spin coated layer. These include resist viscosity, spin speed, spin acceleration and spin time. The viscosity of the resist is proportional to the concentration. The spin speed and acceleration both typically provide thinner layers at higher values. The solvent used for HSQ is MIBK, which evaporates much faster than most other solvents used in resists. After a few seconds the MIBK will have almost completely evaporated leaving the HSQ at its final thickness. Therefore the MIBK requires a fast acceleration to be able to cover the entire wafer and keep the mask thin. To determine the optimal spin coating parameters 12 wafers were spin coated using different resist concentrations, spin speed and accelerations. The time was held constant at 60 s, since increasing the time would not make a difference since most of the resist will be spinned away in the first few seconds. The thickness of the resist was measured using an ellipsometer, and the results can be seen in figure 3 and 4. When using the ellipsometer, a mean of eight individual measurements were taken to get a more precise result. Looking at a diagram of the mean square error (MSE) at the different measure points, also makes the necessity of this type of measurements obvious.

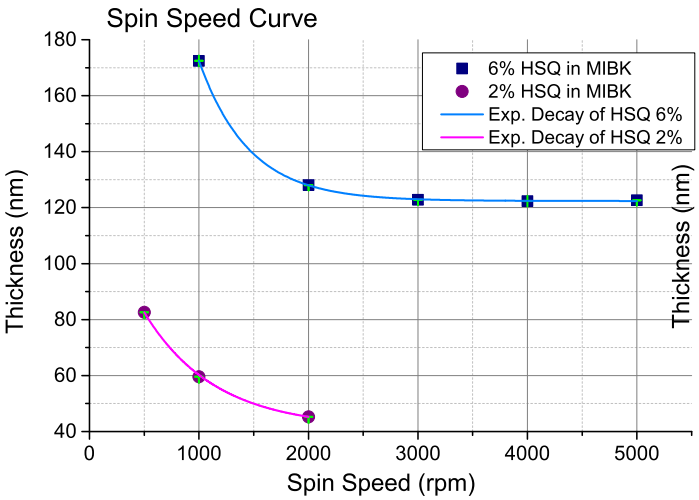


Figure 3: HSQ thickness as a function of spin speed, measured in an ellipsometer. The acceleration was 1000 rpm/s and the time was 60 s.

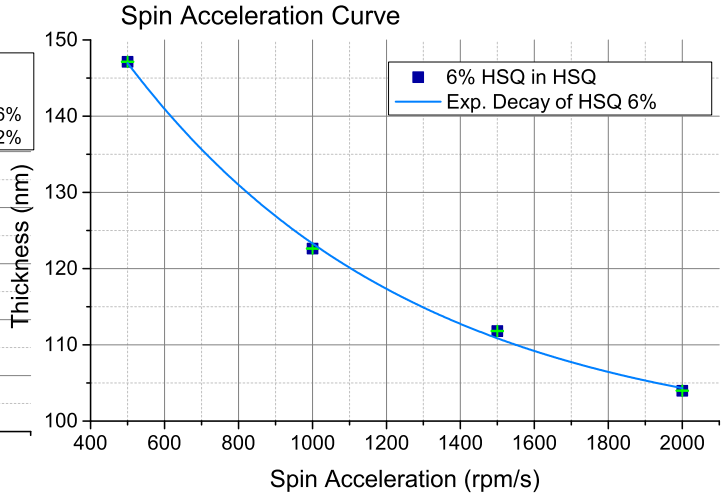


Figure 4: HSQ thickness as a function of spin acceleration, measured in an ellipsometer. The speed was 5000rpm and the time was 60 s.

The figures 3 and 4 shows the datapoints measured along with a fit of an exponential decay. It is obvious from the figures that a higher acceleration or speed generally results in a thinner film. The thickness reduction is an exponential decay, resulting in an approximate minimum thickness. For 6% HSQ this value is approximately 120 nm with constant acceleration, but it is approximately 100 nm with a constant speed. This indicates that acceleration has a higher impact on the final thickness, which is consistent with the fact that the MIBK evaporates very fast resulting in the viscosity rising very quickly in a short time. If the acceleration is then too slow, the final speed will not have much impact on the thickness since the HSQ is too thick already. The 2% HSQ exhibits the same tendencies as the 6% resist.
From this the parameters for the following spin coatings were chosen. For 6% HSQ a speed of 5000 rpm and an acceleration of 3000 rpm/s were chosen. For the thinner 2% HSQ a speed of 2000 rpm and an acceleration of 1000 rpm/s were used.

2.1.2 Surface Roughness

When a pattern in the resist is transferred to a substrate by etching, the sidewall roughness and line edge roughness in the resist will also be transferred to the substrate. For some special applications it is not favourable with a large surface roughness, e.g. nano imprint lithography, where the surface roughness is transferred as well. To compare the roughness of HSQ to other negative resists, the surface roughness is measured in an AFM (Atomic Force Microscope) on wafers spin coated with HSQ fox 15, AR-N7520 and AZ nlof 2020 respectively.

After that, the resists were exposed in white light and hard baked at 250 °C in 10 minutes, and then measured again. Though the white light exposure does not have exactly the same effect on the resist as E-beam exposure, the test shows what type of effect an exposure will have on the resist.

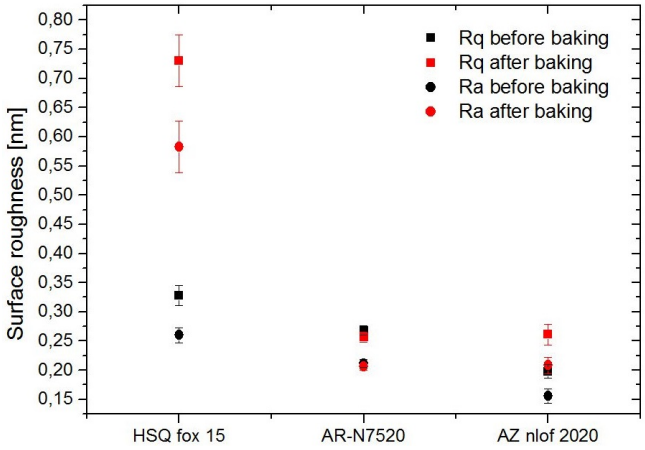


Figure 5: Surface roughness measured for three different negative resists: HSQ Fox 15, AR-N7520 and AZ nlof 2020 respectively before and after exposure in white light and hard baking. The surface roughness is measured in a AFM with contact mode

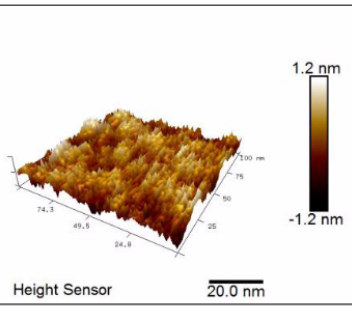
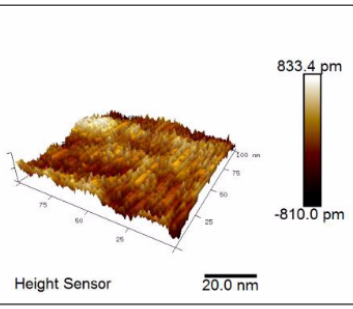
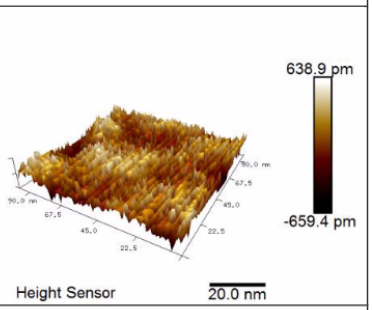
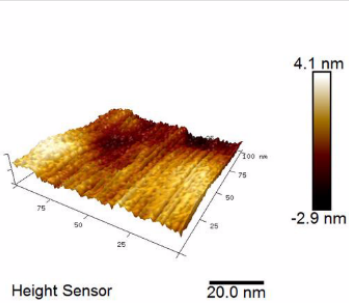
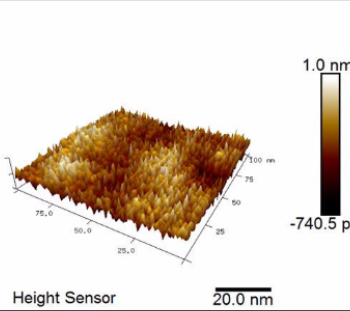
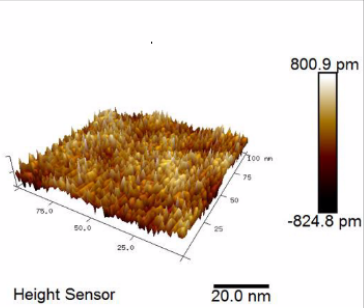
Spin coating, softbaking			
Resist	HSQ fox15	AR-N7520	AZ nlof 2020
3D view of scanning region			
Rq (nm)	0.328	0.268	0.198
Ra (nm)	0.260	0.212	0.156
Exposure in white light (all three resists are sensitive to UV light), and hard baking (250C) for 10min			
3D view of scanning region			
Ra (nm)	0.730	0.256	0.261
Rq (nm)	0.582	0.206	0.208

Figure 6: Table comparing the three resist: HSQ, AR-N and AZ before and after white light exposure and hardbaking at 250 °C, in 3D surface roughness. The 3D images was made with an AFM mapping in contact mode

The results from the AFM mapping and analysis can be seen in figure/table 6 and figure 5. It is seen from the Ra-values, which is the arithmetic mean of the measured roughness, and the Rq values, which is the root mean

squared, that all the resists have rather low surface roughness, below 0.5 nm. Although HSQ has the highest roughness of the three, the roughness is still very low for a resist, and it is preferred because of its high resolution. It is also seen that HSQ's roughness increases a lot after the exposure/hard baking, this means that one should take care when transferring the pattern of HSQ, since if its done under a high temperature, the roughness will increase. It can also be seen in the 3D-mapping in table 6, that the resist change structures after exposure and hard baking. AR-N and AZ gets sharper peaks in the structure after exposure, while HSQ is doing some sort of self assembly, which can be seen from the lines in the structure in the 3D-mapping. This self-assembly might be the reason that HSQ's surface roughness increases a lot after exposure.

2.2 E-Beam Lithography

EBL is a writing technique for high definition nanoscale patterns. It consist of scanning with an electron beam on a electron sensitive resist, for a negative resist unexposed areas will be removed during development.
The limiting factors of the resolution in EBL, which we can change, are properties of the resist and back- and forward-scattering of electrons.
Forward scattering is an electron-electron interaction, an inelastic collision where energy is lost to another electron in the resist. This contributes to the broadening of the beam diameter in the resist. Back scattering is an elastic collision where kinetic energy is conserved. Due to the interaction with the nuclei of the substrate, backscattered electrons deflects with higher angles than forward scattered electrons, resulting in energy being dispersed in a wider area in both the mask and the substrate. Because electrons scatters back into the resist, close features are overexposed - this is called proximity effect. This proximity effect builds "bridges" between structures close to each other in a negative resist, these bridges can for example be seen on the 20 nm lines on the SEM picture from the long lines measurements in figure 7, made in section 2.3.2.

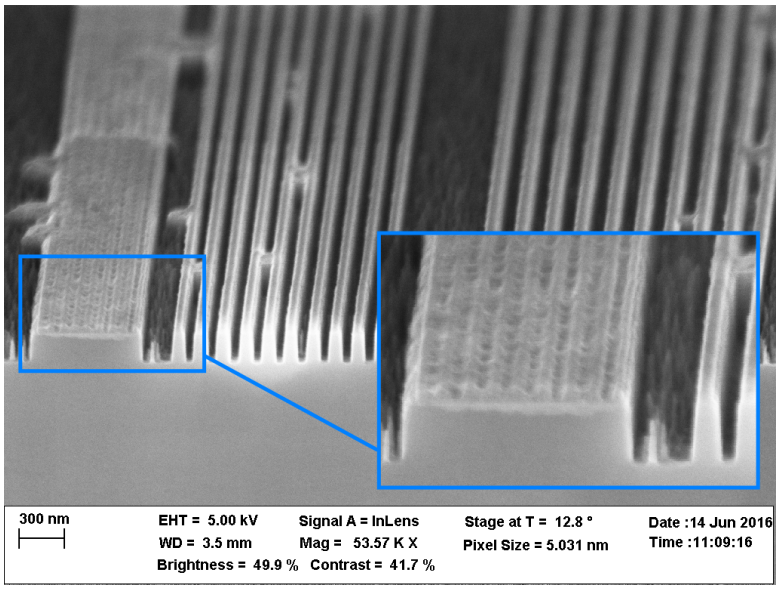


Figure 7: Long lines etching profile for 20 nm, 30 nm and 40 nm wide lines. The zoom shows an example of the proximity effect having widened the mask lines from below, eventually creating a whole mask surface, which does not allow etching of the substrate below.

Another factor that contributes to the proximity effect, is the secondary generation electrons. These electrons contributes the least to the broadening of the beam diameter. The electron beam writer used is a JEOL JBX 9500 in DTU Danchip, that can accelerate 100 keV energy electrons from a thermal field emitter, which emits electrons from a conduction material by a combination of heating and strong electric field.

To find the optimal exposure dose, a dose test was done where the exposure dose was increased with 2000 $\mu C/cm^2$ each step. The optimal dose was found to be 30.000 $\mu C/cm^2$ for the 6% HSQ from figure 8 seen below. Therefore in the following section the dose was set to 30.000 $\mu C/cm^2$ for the 6% HSQ, for the 2% HSQ smaller doses were used.

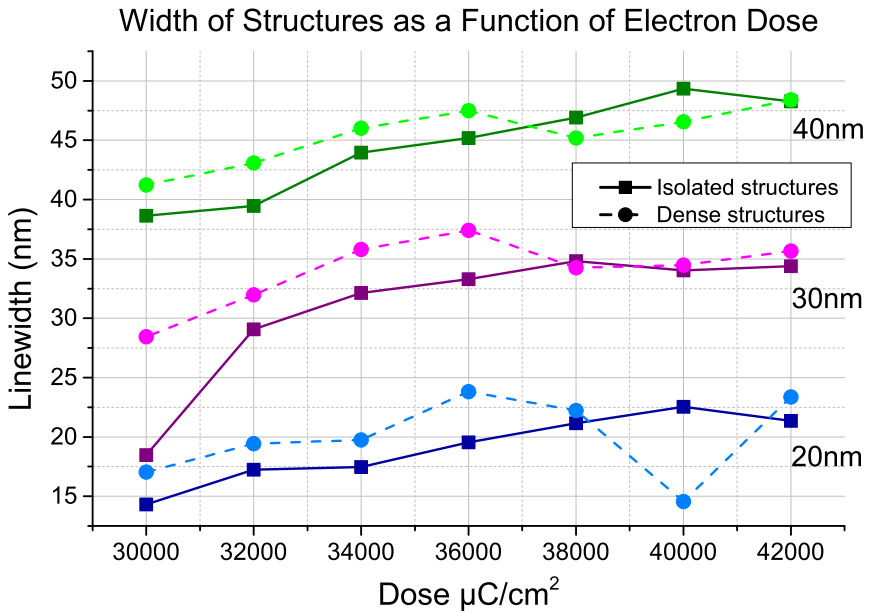


Figure 8: Exposure dose test made on the 6% HSQ, for isolated lines and dense lines. The width's were measures after development in a SEM.

2.2.1 Optimization with 2^3 Factorial Experiment Design

To optimize the process, we used the 2^3 factorial design to analyse which parameters have the biggest influence separately, and combined, on defining the size of the structures on a HSQ resist. The parameters that were analysed, were soft baking time, development time and development temperature, which each is tried at two levels - high (+) and low (-). The possible combinations for the experiment is shown below in table 2.

Treatment combination	I	A	B	AB	C	AC	BC	ABC
(1)	+	-	-	+	-	+	+	-
a	+	+	-	-	-	-	+	+
b	+	-	+	-	-	+	-	+
ab	+	+	+	+	-	-	-	-
c	+	-	-	+	+	-	-	-
ac	+	+	-	-	+	+	-	-
bc	+	-	+	-	+	-	+	-
abc	+	+	+	+	+	+	+	+

Table 2: Factorial Effect: A = Soft baking time which can be 2 min (-) or 4 min (+), B = Development time which can be 2 min or 4 min and C = Development temperature which can be room temperature (RT) or 35 °C.

To do the factorial design analysis, 2 wafers were spin coated, as per the optimal parameters earlier found. These two wafers were soft baked for respectively 2 and 4 minutes. Both wafers were then exposed by the optimal dose found earlier, and were then cleaved in four pieces each. Each piece was then developed in NaOH for either 2 or 4 minutes, by either room temperature or 35 degrees. The line width of the structures were then measured in a SEM, and ANOVA (Analysis Of Variance) tables were constructed for both the dense structures see table 3, and the isolated features (IF), see table 4.

Source of Variation	Effect	Sum of Squares	Degrees of Freedom	Mean Square	F_0	P-Value
Softback time (A)	1.8333	20.1667	1	20.1667	5.4845	0.0325
Development (B)	-3.5	73.5	1	73.5	19.9887	0.0004
Development (C)	-5.5	181.5	1	181.5	49.3598	< 0.0001
AB	0.1667	0.1667	1	0.1667	0.04533	0.8341
AC	-0.8333	4.1667	1	4.1667	1.1331	0.3029
BC	0.5	1.5	1	1.5	0.4079	0.5321
ABC	0.8333	4.1667	1	4.1667	1.1331	0.3029
Error		58.8333	16	3.6771		
Total		323.8333	23	14.0797		

Table 3: Analysis Of Variance, ANOVA for dense lines.

Source of Variation	Effect	Sum of Squares	Degrees of Freedom	Mean Square	F_0	P-Value
Softback time (A)	1.1667	8.1667	1	8.1667	3.3793	0.0847
Development (B)	-1.3333	10.6667	1	10.6667	4.4138	0.0519
Development (C)	-3.5	73.5	1	73.5	30.4138	< 0.0001
AB	-0.8333	4.1667	1	4.1667	1.7241	0.2077
AC	1	6	1	6	2.4828	0.1347
BC	1.1667	8.1667	1	8.1667	3.3793	0.0847
ABC	0.3333	0.6667	1	0.6667	0.2759	0.6066
Error		38.6667	16	2.4167		
Total		150	23	6.5217		

Table 4: Analysis Of Variance, ANOVA for isolated lines.

In order to optimize the process to get the smallest and highest contrast structures, the process was optimized based on the analysis from the ANOVA tables in figure 3 and 4. It is seen from these tables, that in order to get smaller structures, the soft baking time should decrease, the development time should increase and the development temperature should increase. However, if the temperature increases, the silicon will start to etch away, which will make the structures more rough, which goes against the other aim of the optimization process. Also increasing the development temperature will have a huge influence on the final result, which is difficult to control. The development time can't be increased too much either, as the dark erosion will start to etch away the exposed structures and the swelling effect will reduce resolution of the structures. Also, the soft baking time can't be reduced to nothing, as it is needed in order to remove residual MIBK solvent from the resist. Therefore the process parameters for the optimization was 1 and 2 minutes soft baking time, as well as 4 and 6 minutes development time, where the development temperature were held at room temperature. For this process two wafers were spin coated, with a spin speed of 5000 rpm and a spin acceleration of 3000 rpm/s. The two wafers were soft baked for 1 and 2 minutes separately, and both wafers were exposed with a dose of 30 000 $\mu C/cm^2$ and a current of 1.7 nA. After the exposure, both wafers were cleaved in two pieces, and developed almost instantly after exposure, whereas each piece were developed in respectively 4 and 6 minutes. The structures were then measured in a SEM, which yielded the following results for the optimized process, see figure 9.

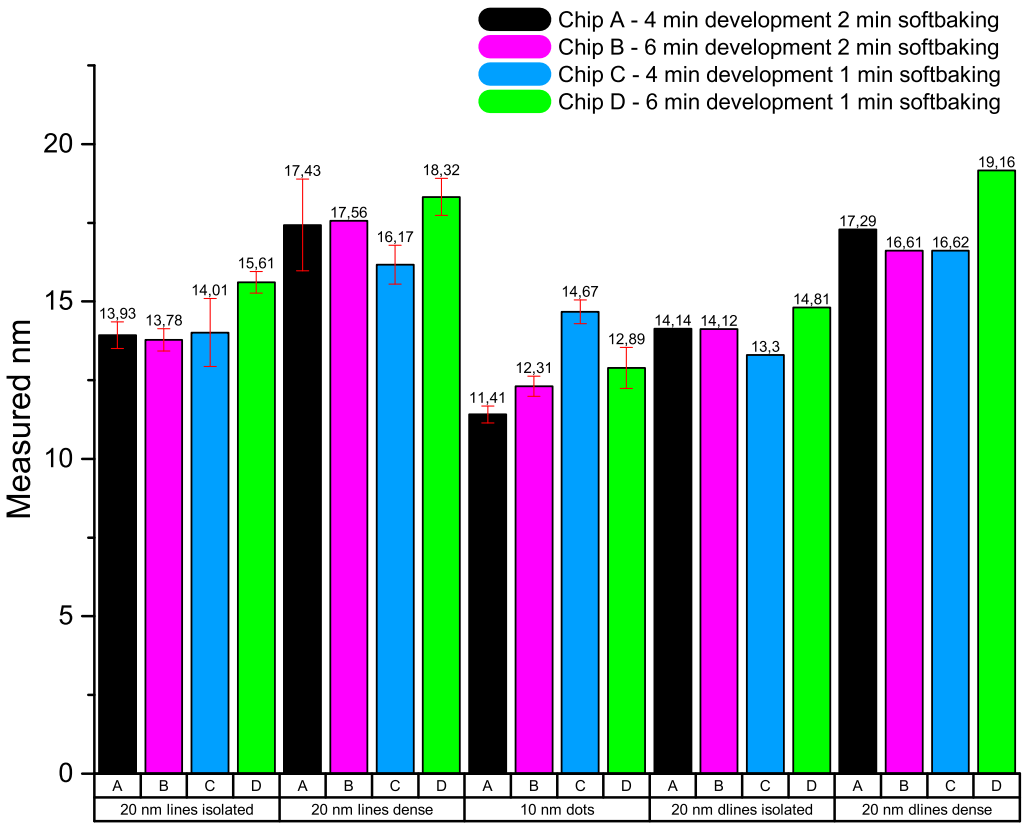


Figure 9: Measured feature size, diameter for dots and width for lines, of structures written on wafers, with different softbaking times and development times. The feature sizes were measured in a SEM, where the mean of the values have been taken, and the standard deviation has been used as the error.

It is seen from the bar plot in Figure 9, that chip C which was soft baked in 1 minute, and developed in 4 minutes, has the smallest features. The difference is minuscule in the isolated features, which corresponds to the low effect estimates in the ANOVA table in figure 4. But for the dense structures it is clearly seen in the 20 nm dense line structure, that the feature size has been reduced by a whole nanometer. That chip C has smaller features than chip D, means that the combined effect of these parameters have been underestimated, at these values the combined effect increases the line width quite a lot. It is also seen, that the ANOVA optimization didn't work on the dot features, which is to be expected, since the ANOVA was made, using the line width of the dense and isolated features, and not of the dots. Besides getting smaller features, another aim of this project was to get higher contrast features, to evaluate whether the features were less rough, pictures were taken by a SEM.

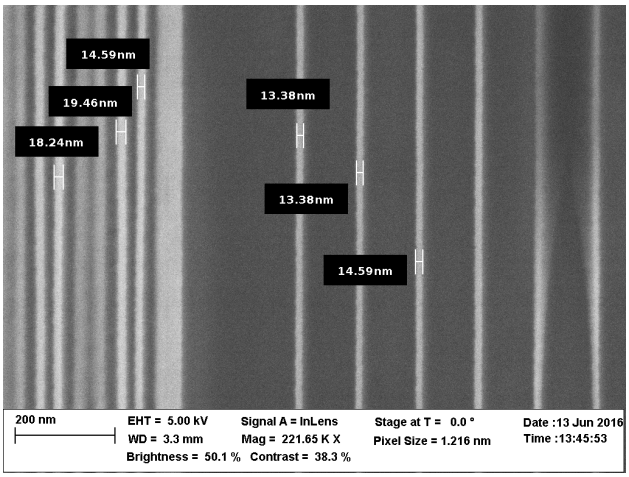


Figure 10: Chip A - Before ANOVA optimization

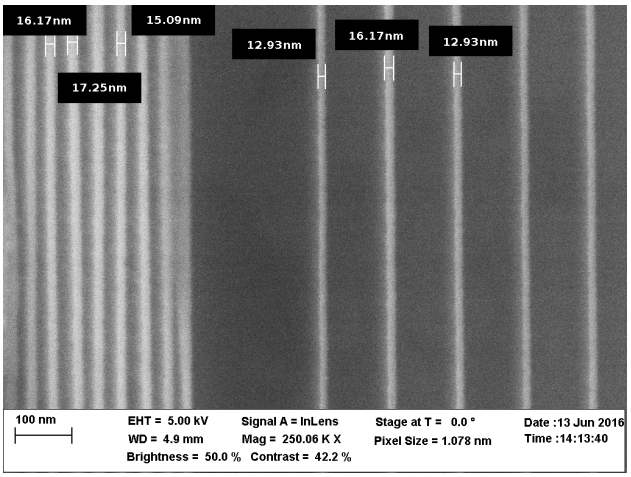


Figure 11: Chip C - After ANOVA optimization

Figure 12: SEM images of 20 nm lines structures, of the wafers before and after the ANOVA optimization. Before optimization the softbaking time were 2 minutes, and the development time were 4 minutes. After the optimization the softbaking time were 1 minute and the development time were 4 minutes.

It can be seen from the SEM-images of the 20 nm lines in figure 12, that the dense lines before the ANOVA optimization in figure 10, is much more rough (there is more residue, and the structures are collapsed) than the dense lines after the optimization, seen in figure 11. This is quite an important result for the transfer of the pattern from the mask, into the substrate, as any roughness in the pattern also would get transferred. However, most structures won't be as simple as isolated and dense lines, therefore, this recipe was also tested on a more advanced structure.

2.2.2 Complex structure

For the advanced structure, a new wafer was spin coated with 6% HSQ at 5000 rpm and 3000 rpm/s. The wafer was soft baked and developed, according to the best results from the ANOVA optimization (1 min soft baking time, and 4 min development time). The advanced pattern was a capacitor setup, widely used in accelerometer. This pattern can be seen in figure 13, where it is seen that the pattern is repeated for capacitors with width, and space between lines of respectively 15, 20 and 30 nm.

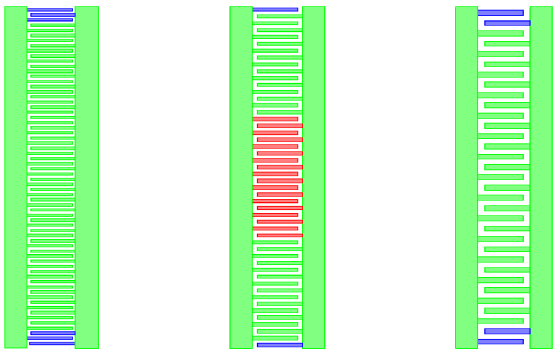


Figure 13: Capacitor design for EBL exposure, colored areas represent different doses due to proximity error correction.

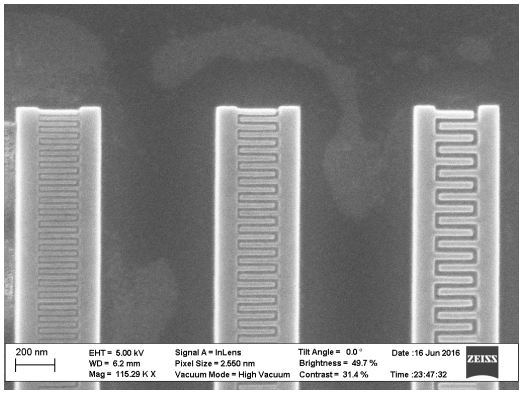


Figure 14: SEM image of capacitor design in 6 % HSQ-resist after exposure

After the exposure and the development, the structure was imaged in a SEM, this image can be seen in figure 14. The exposure was actually done both with and without proximity error correction (the differently colored areas in figure 13, represents the different doses from the PE), and with a bias, but all these yielded the same results, since the exposure dose was so high ($30.000\,\mu C/cm^2$) compared to the dose difference done by the PE ($(500\,\mu C/cm^2$). It is seen from the image in figure 14, that with the optimized process, even advanced structures,

like the ones widely used in modern accelerometers can be made, with a feature size of down to 15-20 nm without an increase in roughness. These are quite good results, when it is kept in mind, that the resist layer was app. 100 nm thick. In order to try to get a even higher resolution, the 2 % concentration was tried as well.

2.2.3 Further Optimization with Thinner Resist

A wafer was spin coated with 2% HSQ with the optimal parameters found in the spin coating section. The wafer was softbaked at 1 minute, as the short soft baking gave the optimal results in the previous optimization. The wafer was exposed with a lower current 0.17 nA and a lower dose 20.000 µC/cm^2, as the resist was thinner (45 nm), and therefore needed a lower exposure to cross link. After exposure the wafer was cleaved in 4 pieces, and each were developed separately at 0.5 min, 1 min, 1.5 min and 2 min respectively. The development time for the thinner resist was shorter, since less time was needed to develop the features in a thinner resist, and too much time would etch the structures away, due to dark erosion.

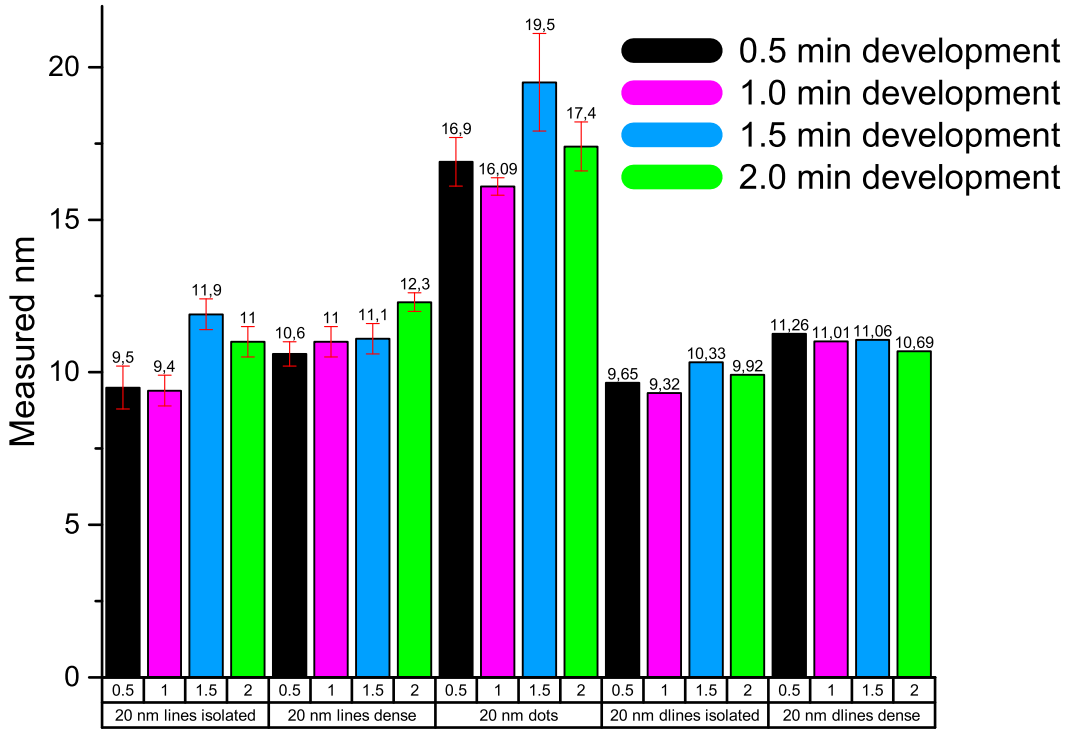


Figure 15: Measured feature size, diameter for dots and width for lines, of structures written on 45 nm 2% HSQ coated wafers with different development times (which is the second grouping parameter). Values haven been taken as the mean of the measures in a SEM, where the error are the standard deviations.

It is seen in figure 15, that the structures in the 45 nm 2 % HSQ resist coated wafer, has a higher resolution than the structures made in the 100 nm resist coated wafer earlier. Structures with feature dimensions of about 10 nm have been obtained, whereas the critical dimensions for the 100 nm resist, was over 13 nm. It is also seen, that the feature size reduces a little with a shorter development time, for the 2 % concentration HSQ.

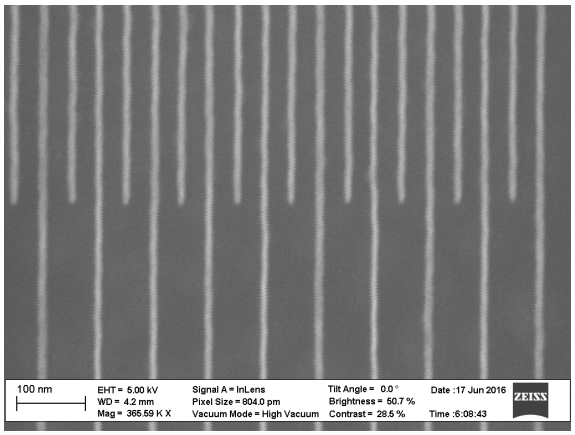


Figure 16: 20 nm dlines for 2 % HSQ coated wafers, that were developed for 0.5 min after exposure.

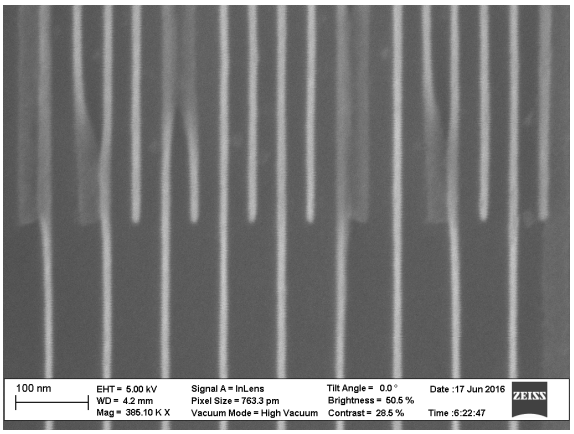


Figure 17: 20 nm dlines for 2% HSQ coated wafers, that were developed for 2 min after exposure.

Besides the features getting smaller, the structures also get a higher contrast with a shorter development time, which can be seen from the SEM images in figure 16 and 17. It is thus seen, that for getting a higher resolution, the 2 % concentration HSQ is far better than the 6 %, as the structures are quite a lot smaller, even below 10 nm, and still has a high contrast.

2.3 Pattern Transfer

2.3.1 Selectvity of HSQ

The selectivity is the ratio between the etch rates in the substrate and the mask.

$$\text{Selectivity} = \frac{\text{Etch rate in substrate}}{\text{Etch rate in mask}} \tag{2}$$

This is important when deciding the thickness of the mask, since a thinner mask can have higher resolution structures, but will get etched away if a deep structure is required. The etch depth on two of the wafers were measured from scratching a coated surface, plasma etching of the wafer and SEM pictures taken of the cross-section. Which is a rough estimation of selectivity. The results are given in table 5.

	Etched depth in Si	Etched depth in HSQ mask	Selectivity
w903	5.429 µm	65 nm	93.9
w904	4.678 µm	56 nm	70.4

Table 5: Results of selectivity measurements made on two 6 % HSQ coated wafers.

To find the meaning of this a small calculation is made. Given an HSQ layer of 100 nm the deepest etch possible with the current selectivity is $d_{max} < 100\text{nm} \cdot 80 < 8\,\mu\text{m}$. This height is without the precaution of having at least 20% left of the mask. Because during development 20% of the total thickness is lost due to dark erosion. When making the selectivity calculations several things must be taken into account. Scratches across an entire wafer surface are quite large structures, which means a shallow, dry, bosch etch recipe was used. For the smaller structures etched in the rest of this section, an etch recipe with a smaller etch rate was used, since the structures were in the nano-range. Selectivity goes down with the etch rate, so for the remaining etches in this report, the etch rate that is much lower than the ∼80 found above.

2.3.2 Reactive Ion Etching

With the mask pattern defined the next step is etching. The silicon was etched using an ASE, which performs reactive ion etching using high density plasma. The recipe used is a Bosch process performed at room temperature with a deposition phase of 3 s (C4F8 50sccm, and coil power 500 W), and an etching phase of 5 s (C4F8 50sccm, SF6 50sccm, coil power 350 W and platen power 30 W). The processing pressure was set to only 10 mTorr to reduce the lateral etching, which is the etching of the sidewall in a perpendicular direction to the silicon surface.

The total time of the process was 2 min.
Two different patterns were etched. Firstly a wafer was made with 1 cm long lines of different widths. This wafer was cut in half to be able to see the etching profile. From the cross section SEM picture of the long lines seen in figure 19, it is seen that wider openings in the top results in deeper trenches. This is because the etch rate depends on the local opening area in the mask. The wider the mask line area, the higher the etch rate, which leads to a deeper trench. This is called the loading effect and can be seen in figure 18. This is done for HSQ, which is a negative resist.

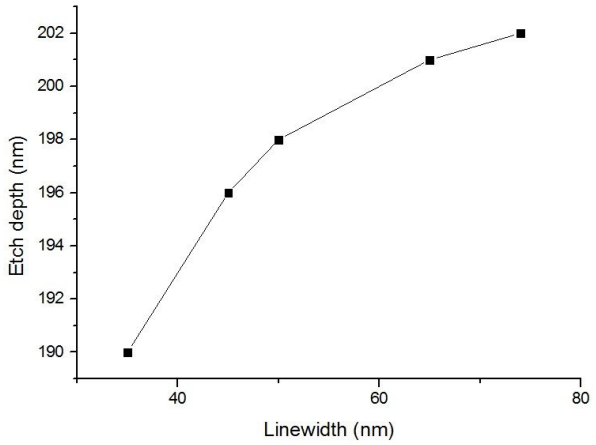


Figure 18: The figures describes the relation between the width of the line in the mask and the etch depth. wider lines creates smaller gaps, which results in a deeper trench. The etch depth is proportional to the etch rate.

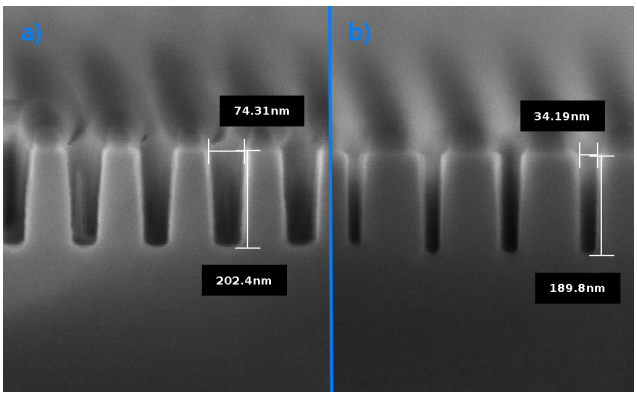


Figure 19: Cross section of the 50 nm long lines made in 2 % HSQ with a dose of 20.000 µC/cm^2 (a) and a dose of 28.000 µC/cm^2 (b).

Secondly the small structures described in the end of the previous section were etched. These structures were made in a 45 nm thick resist. Figure 20 shows the etching result obtained. The 20 nm dense lines have a high resolution, with no collapsed walls and very little residues. Showing that the width of the lines are around 10 nm and have anisotropic etching profiles, with visible but not prominent scallops.

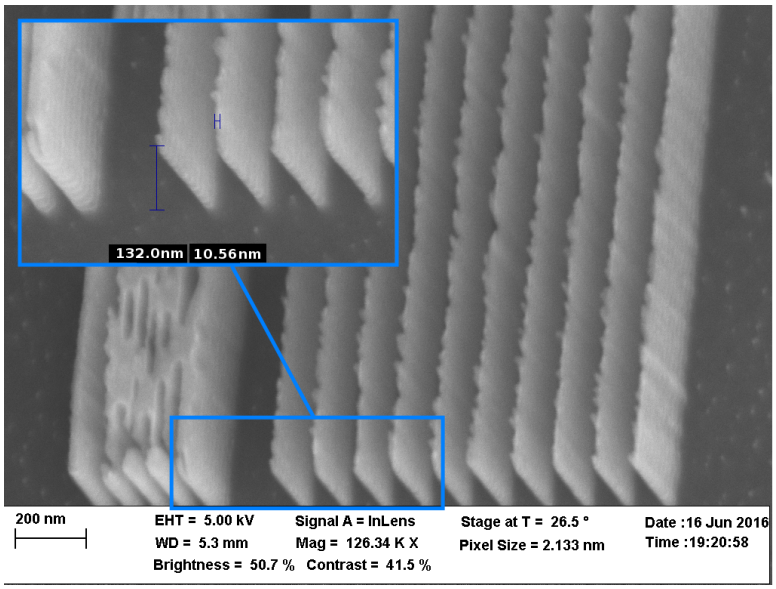


Figure 20: SEM picture of 20 nm dense lines after etching on the 45 nm 2 % HSQ with a dose of 20.000 µC/cm^2 , with a zoom in on the edge, where a slight scallop structure can be seen.

3 Conclusion

From this report, it can be concluded that in order to get the highest resolution of the structures, 2% HSQ-1541 should be spin coated with a relatively high spin speed (2000 rpm) and acceleration (1000 rpm/s), soft baked for as short a time as possible (1 min), e-beam exposed with a low current (0.17 nA) and a relatively low dose (20.000 $\mu C/cm^2$) and developed for a short time (0.5-1 min) in NaOH. With the parameters used in these experiments, sub 10 nm structures have been obtained with the 2% HSQ.
6% HSQ might be more desirable, depending on the needed depth of the etching, as a problem with the sub 50 nm 2% HSQ masks, is that a deep etch would cause erosion in the mask. With the parameters used in these experiments (spin speed: 5000 rpm, spin acceleration: 3000 rpm/s, soft bake time: 1 min, e-beam current: 1.7 nA, e-beam dose: 30.000 $\mu C/cm^2$, development time: 4 min) , the highest resolution obtained on a 100 nm thin resist of 6% HSQ, has been 13 nm for isolated lines. HSQ patterns were successfully transferred into silicon with reactive ion etching. With a maximum etch depth around 300 nm in the 45 nm resist. This demonstrates good selectivity of HSQ in etching process, which will be promising in nano-fabrication.

4 Outlook

For further investigation experiments should be reproduced, to test reliability of the best results. This would also provide more data on the use of HSQ, which is not well documented in DTU Danchip. To obtain structures with higher resolution different substrates might be used fx. silicon dioxide (SiO_2), which will reduce the backscattering of electrons. For 2% HSQ masks another factorial experiment design should be carried out to obtain the parameters for the best result.
The high resolution mask structuress could be used to transfer pattern to Gallium Arsenide (GaAs), magnetic material or thin metals to make superconducting materials. Furthermore small HSQ structures could be transferred into metal or magnetic material, which shows promising properties for quantum transport and bit patterned media for high density hard disc structures.

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Process flow

Objective
Batch name: high resolution nanostructures definition with electron beam lithography
Thin HSQ resist will be used as electron beam resist, different processing parameters will be studied and compared.

Substrates									
Substrate	Orient.	Size	Doping/type	Polish	thickness	Box	Purpose	#	Sample ID
Silicon	<100>	4"	p	SSP	525±25µm		Test wafers	22	T1-T2

Step Heading		Equipment	Processing parameters	Comments
1	Pretreatment			
1.1	Soft backing	Hotplate	80°C for 10 min	
2	Spin coating			
2.1	Coating wafers	Spin coater Manual standard (E5)	Resist: HSQ XR-1541-006; Spin time: 60 sec; Spin speed: 1000 - 5000 rpm; Acceleration: 500 - 4000 rpm/s; Soft backing: 80°C for 1 min, 2 min or 4 min	HSQ XR-1541-006 is easy to evaporate, an acceleration of 2000rpm/s can give thickness around 100nm. A thinner layer is aimed for a higher resolution.
2.2	Characterization	Ellipsometer VASE (B1)	9 point SiO2 measurement 55-60-65 degrees. Using model of SiO2 (Sellmeier)	Average thickness and mean square error (MSE) will be measured, and spin curve obtained.
3	E-beam exposure			
3.1	E-beam exposure	E-beam writer Jeol JBX 9500 (E2)	100kV Beam current: 2nA; 0.2nA; Step size: 5nm (single pixel line); Doses: 20000 - 42000 µC/cm^2.	Both dense structures and isolated structures will be designed. Pattern will be repeated on the 4 different positions on wafer surface.
4	Development			
4.1	Development	E-beam Fumehood (D3)	Developer: NaOH solution (1% NaOH and 4% NaCl in water); Rinse: DI water for 60 - 90s; Developing temperature: room temperature, 35 °C; Drying: Nitrogen gun.	Wafer cleaved into 4 pieces, developed in different conditions.
5	Measurement			
5.1	Inspection	SEM supra 2, or SEM supra 3 (C1)	5kV, inlens mode. Surface or cross section inspection.	Structures with different doses and developing conditions will be inspected and compared.
6	Pattern transfer			
6.1	Etching	ASE (B1);	Recipes: pxnano2 (ASE)	Bosch process in room temp., depsotion 3s (C4F8 50sccm, and coil power 500W) and etching 5s (C4F8 50sccm, SF6 50sccm, coil power 350W and platen power 30W), pressure 10mTorr, time 2 min.
6.2	Inspection	SEM supra 2, or SEM supra 3 (C1)	15kV, inlens mode. Surface or cross section inspection.	Etching profile will be compared.

Figure 21: