Report on

RAPID THERMAL PROCESSING ON SILICON/NANOFABRICATED STRUCTURES

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1   GENERAL DESCRIPTION

1.1   Contextualization and Objectives

Rapid thermal processing, RTP, is the given name to any process that implies elevating the temperature of a given material, mainly semiconductors, to high values during short periods (minutes or even less) [1], [2]. It can be used, for instance, to form metal nitrides (RTN), for selenization, post-ion implantation annealing, dopant activation, thin-film oxide layer growth (RTO) and annealing (RTA) [1], [3]. This report summarizes the experimental work carried out on a research rapid thermal processor (RTP AS-Premium, serial number AS0415C4 - 8177, from ANNEALSYS). It aims to demonstrate how it can be used as a multi-functional and versatile microfabrication tool, within specific process windows for each process type, using silicon (Si)/nanofabricated Si structures.

1.2   Rapid thermal processor: Set-up

The RTP tool is characterized by a top and bottom halogen lamp-configuration (2×14 lamps), as shown in Figure 1. Moreover, the tool offers an optical pyrometry system for temperature measurement, not requiring any contact with the wafer. Besides, the chamber is enclosed by two quartz-windows and it's only connected to two external vacuum pumps, to a gas inlet and the loadlock – in front of the chamber, separated by the gate valve. While processing, the valve is closed, preventing any disturbance; it is only opened to exchange the substrates when both chamber and loadlock are under vacuum. The substrate transfer is possible due to the mechanical, retractable arm.
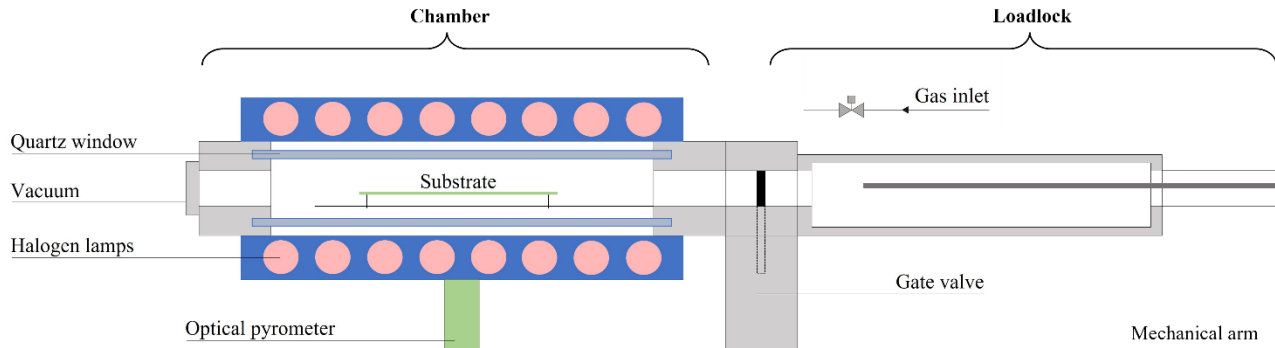
Figure 1 - Schematic representation of the rapid thermal processor set-up profile view. The substrate (in green) rests on top of three quartz pins, supported by a quartz holder (in black). The drawing is not to scale.

It is also important to mention the tool can function under two distinct modes – power and temperature control modes. In other words, using power control mode, the tool is programmed to fix the lamp's power at a specific value (%) and consequently, the temperature inside the chamber varies with time; using the temperature control mode, the tool is programmed to vary the lamps' power to maintain the temperature stable and constant inside the chamber at a previously established value in the recipe.

1.3   Rapid Thermal Processor: Parameters

The rapid thermal processor, with a base pressure of 10^{-6} mbar, is a research tool. As such, there are some parameters and details to consider. These are shown in Table 1.

Table 1 – Rapid thermal processor's allowed parameters and substrates.

Parameters		Allowed
Temperature		up to 1300 ºC*
Process gas	Ar	up to 2000 SCCM
	O$_2$	up to 2000 SCCM
	NH$_3$	up to 2000 SCCM
	5% H$_2$/Ar	up to 2000 SCCM
Pressure	Valve	0º - 100º
	Value	up to 12 mbar
Substrate wafer size		100 mm or 150 mm wafers
Substrate wafer type		Si wafers or Si$_3$N$_4$-coated Si wafers**

* Depending on the processing time.
** The usage of the latter was adopted to prevent harming the tool, further discussed in more detail.

1.4 Experiments Overview

Considering the available process gases, various types of RTP were studied during the experimental work, such as rapid thermal annealing (**RTA**), hydrogenation (**RTH**), oxidation (**RTO**), vacuum (**RTV**) and Black Si smoothing (**Clean BSi**). In addition, it was developed a sequence for tool calibration.

1.5 Test samples

Various test samples were used, which are represented in Figure 2. Type I, II and III samples are 1 cm x 1 cm chips. Type IV and V are 150 mm Si <100> wafers, with grown BSi and without native oxide, respectively. The fabrication process flow can be found in Figure S1.
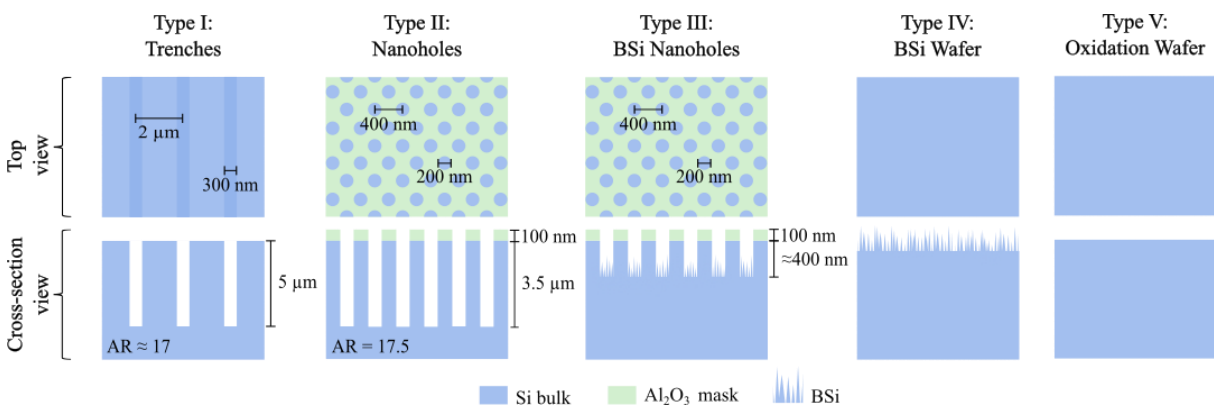
Figure 2 - Schematic representation of the different types of test samples. The drawing is not to scale. The depth in Type III samples varies between 300 nm and 400 nm. The native silicon oxide on Type V samples was stripped before processing, using a BHF with surfactant bath (12% HF with ammonium fluoride etching mixture).

1.6 Type of characterization

The structural characterization was mainly carried out by scanning electron microscopy, although ellipsometry has also been used. The scanning electron microscope (SEM) was a Zeiss Supra 40VP SEM, serial number 4825 and the ellipsometer a variable angle spectroscopic ellipsometry (VASE) M2000XI-210 from J.A. Woollam Co., Inc.

2   RTP: PROCESSES IN DETAIL

2.1   Argon RTA

Rapid thermal annealing sequences were developed and studied using only argon (Ar). Some experiments were repeated in an attempt to establish a reproducibility study. Type I samples were used and processed on top of silicon carrier wafers, with no bonding required. The details for each experiment are presented in Table 2.

Table 2 – Argon rapid thermal annealing experiments and correspondent process parameters.

Sample	Gas	Flow (SCCM)	Temperature (ºC)	Power (%)	Pressure (mbar)	Time (s)	HF dip	Position
RTA 1	Ar	40	1328	80	12	180	No	Up
RTA 2	Ar	40	1305	80	0.18	180	No	Up, covered
RTA 3	Ar	40	1244	80	0.18	60	No	Up, covered
RTA 4	Ar	40	1307	80	0.18	8	No	Up
RTA 5	Ar	40	1308	80	0.18	60	No	Up
RTA 6	Ar	40	1309	80	0.18	180	No	Up
RTA 7	Ar	40	1246	80	0.18	60	No	Flipped
RTA 8	Ar	40	1248	80	0.18	60	Yes	Flipped
RTA 9	Ar	40	1244	80	0.18	60	No	Up

Up = Facing the chamber; **Up, covered** = facing the chamber, covered with an identical (in size) Si chip during the process; **Flipped** = Facing the carrier wafer; **HF dip** = 30s-HF chemical bath, immediately prior to processing.

'RTA 1' experiment aimed to study the influence of RTA sequences on chromium (Cr). As such, type I samples were used, before the Cr hard-mask removal. The results are shown in Figure 3.
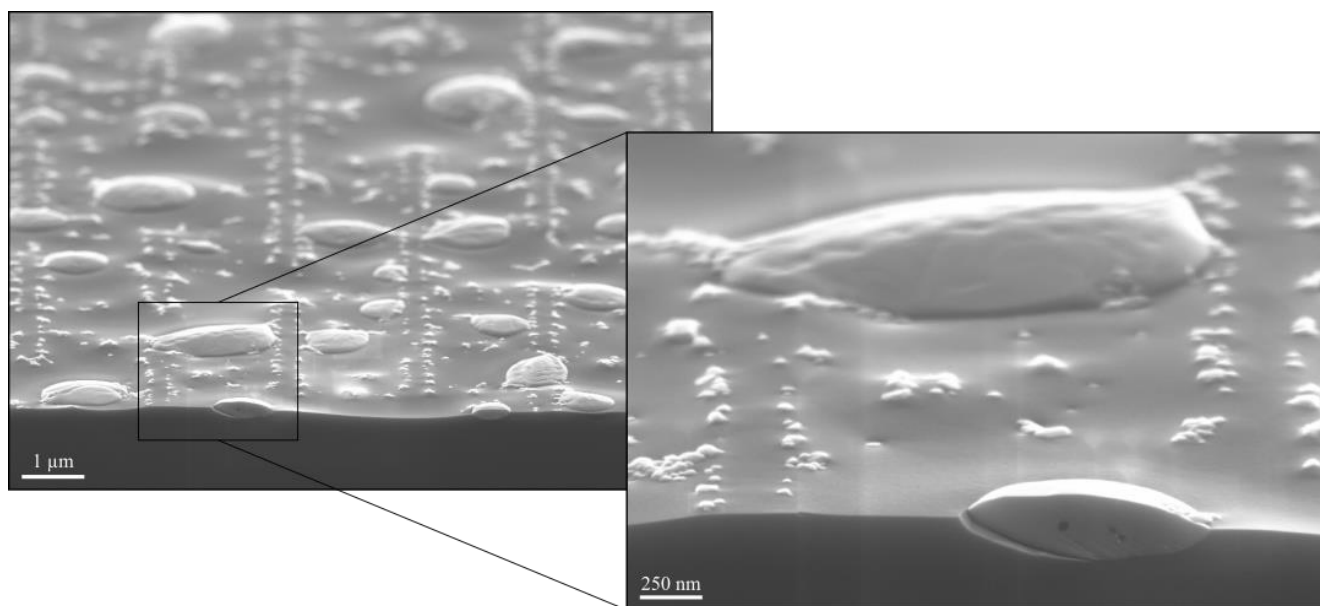
Figure 3 - Effect of rapid thermal annealing on the Cr hard mask at the edge of the sample (non-patterned area) – RTA 1. Cross-section SEM images, 20º tilt and EHT 5 kV.

Additionally, the results from experiment 'RTA 2' are shown in Figure 4, where 3D profile transformation and faceted buried holes formation are achieved, respectively.
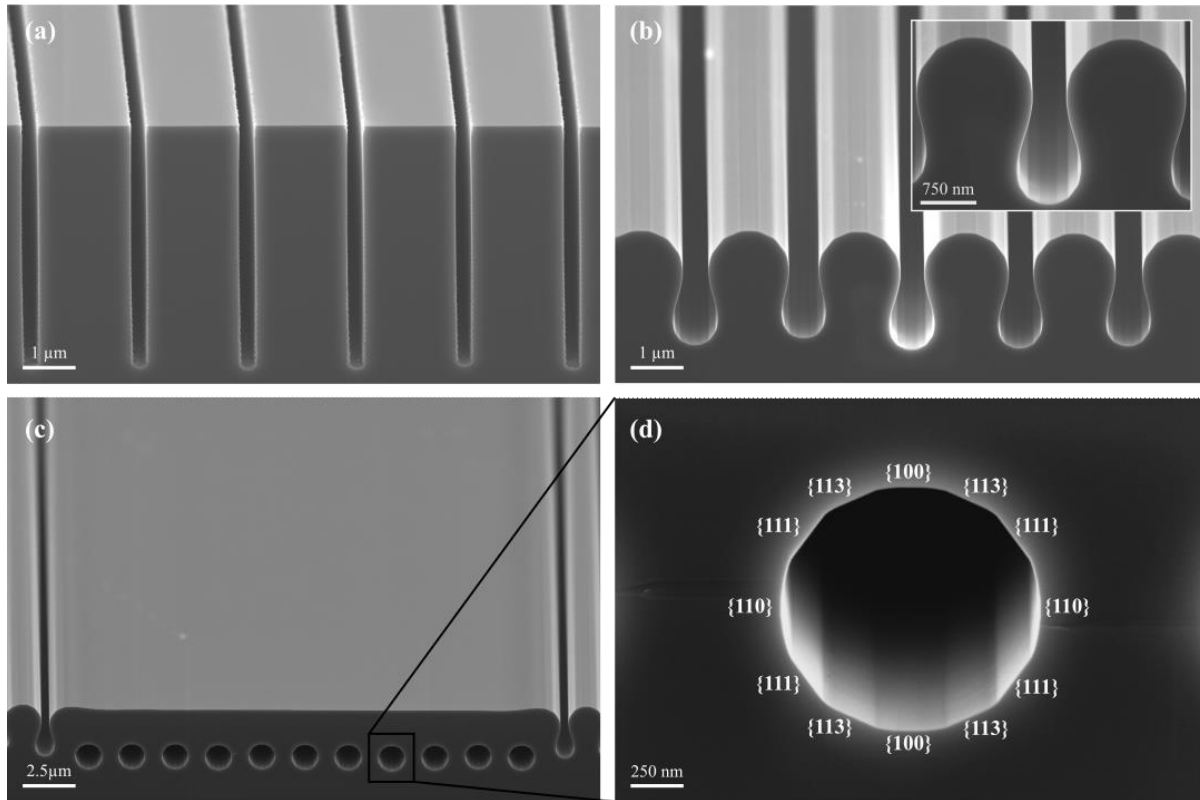
Figure 4 - Transformations achieved by 3-minute RTA (RTA 2). (a): initial state, without Cr mask; (b): post-annealing state, exhibiting 3D profile transformation; (c) area of the post-annealing sample where faceted buried holes were found; (d) faceted buried hole up-close with indication of the corresponding crystallographic directions. Cross-section SEM images, 20º tilt and EHT 5 kV.

Furthermore, the results from experiment 'RTA 3' are visible in Figure 5. In most processed samples, at the edge of the sample, where the patterned area meets the non-patterned area, it is common to find a third type of feature – faceted voids.
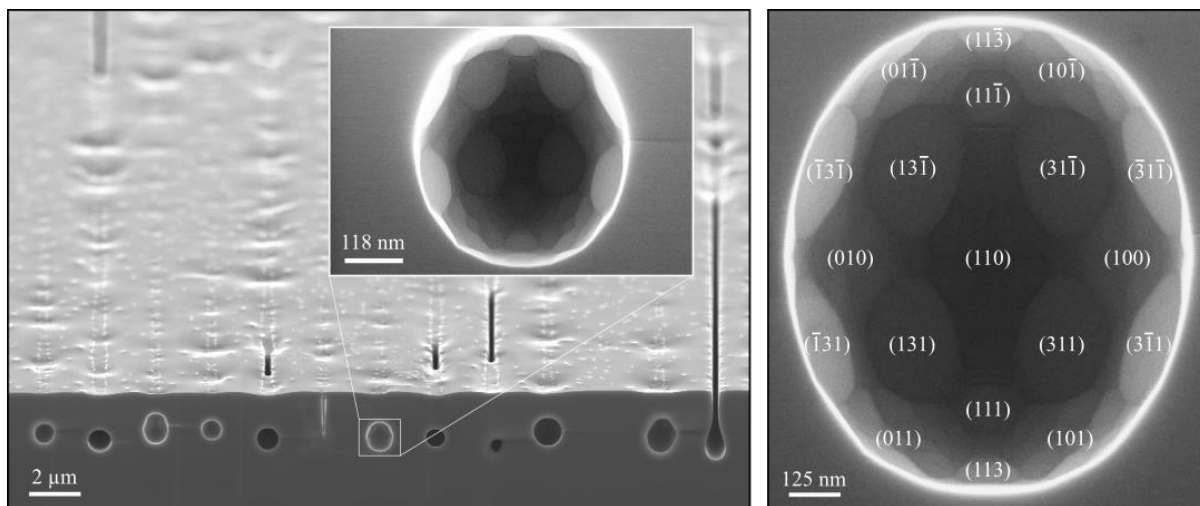
Figure 5 - Faceted void found at the edge of a sample that was annealed (RTA 3), with the indication of Si crystallographic planes on the right. Cross-section SEM images, 20º tilt on both the pictures on the left and 0º tilt on the right, EHT 20 kV.

In addition, a series of subsequential experiments (RTA 4 to RTA 9) was carried out – following the order presented in Figure 6 – in which the Ar gas flow, pressure and lamp power were the fixed parameters and the processing time the differing one. The effect of dipping the samples for 30 s in HF, immediately before RTA processing, has also been tested. Additionally, the influence of keeping the samples facing the chamber ambient *vs* flipping them (i.e., facing the Si carrier wafer) was studied. Consequently, the tool's reproducibility was also investigated.
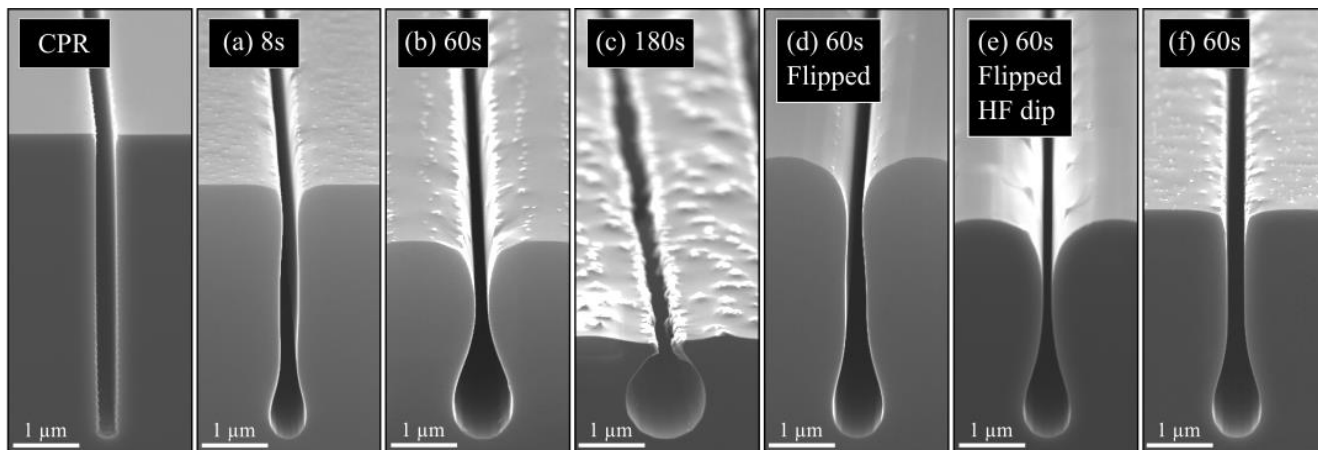
Figure 6 - Influence of process time, prior HF dip and flipping the samples during an RTA process (RTA 4 – RTA 9). All features were aligned at the bottom as a way of comparison, between each other and with the centre point run (CPR). Cross-section SEM images, 20° tilt, EHT 1 kV in (c), EHT 5 kV in (CPR), (e), (f) and EHT 20 kV in (a), (b), (d).

As a first approach, the goal was to understand how to produce the atom migration phenomenon, present in RTA processing in H_2 ambient, using only Ar as process gas instead. The atom diffusion along the Si's surface takes place, so its total surface energy is minimized, causing the rounding of the corners of any existing surface feature [4]–[8], without volume loss [9]. In other words, the Si is reshaped into an ideal, more stable curvature that lowers its surface Gibb's free energy [10], [11].

It was concluded that chromium is not suitable as a masking material for this kind of high-temperature processing, as it crumbles and detaches from the silicon surface, leaving it exposed. For that reason, it was required to remove the mask from all samples before undergoing further testing.

Moreover, three types of structures were obtained due to the Si self-diffusion mechanism through the surface of trench-patterned samples: faceted droplets, buried faceted holes and enclosed faceted voids. The faceted droplets carved into the Si are a product of the deep and narrow trenches' complete 3D profile transformation. The other two types were achieved by reshaping the Si into its equilibrium and most stable form [12]–[14], inducing ESS (empty-space-in-silicon) formation [4], [7] . Same-length facets were found in the droplets, holes and voids and belong to the {100}, {113}, {111} and {110} families of Si crystal planes [12], [13].

Furthermore, keeping in mind the recipes used were in power control mode, it would be expected that the same applied lamp power would lead to identical chamber temperatures for each consecutive experiment. However, a percentage of the energy irradiated from the lamps was being absorbed by the deposited Si instead of being transmitted through the window and absorbed by the sample/carrier wafer. Such was verified - the maximum temperature achieved by the samples dropped 55 ℃ between the first and last experiment in Figure 6, all of them receiving, in theory, 80 % of lamp power. Equally important, the result's lack of reproducibility combined with the discovery of deposited Si on the tool's top quartz-window was evidence enough to suspect other physical

mechanisms were associated with RTA processing. Consequently, it is proposed that not only atom migration is occurring during RTA, but also Si sublimation from the surface, as well as Si 'burning'. This last phenomenon refers to the reaction between unwanted oxygen inside the chamber and silicon atoms from the sample's surface, promoting the formation of volatile silicon monoxide (SiO). Consequently, this causes the silicon surface to be etched and as a result, a pure Si surface is left behind.

As a final remark, this set of experiments revealed that rapid thermal processing should **only** be performed using sequences under '**temperature control' mode**. Thus, major temperature fluctuations during processing can be prevented and **temperatures above 1300 ºC avoided**. Nonetheless, **'power control mode'** can be used for **short-period** RTP sequences (a few seconds) or to **heat up the chamber** before the process itself initiates (initial standard steps included in the recipes). Both high and low-pressure processing did not seem to induce any harm to the tool.

2.2 RTH

Rapid thermal hydrogenation (RTH) sequences were developed and their effects on silicon were studied. The results were also compared with the ones obtained using equivalent Ar RTA sequences. Type II samples (before undergoing the final Si etch step) were used and processed on top of silicon nitride (Si_3N_4)-coated silicon carrier wafers, without any bonding.

It is worthwhile mentioning, this set was performed under the 'temperature control' mode. This mode was revealed as a better option as the temperature did not suffer any significant changes throughout the process, as opposed to what was verified using the 'power control' mode. The details for each experiment are presented in Table 3.

Table 3 - Rapid thermal annealing and hydrogenation comparison experiments and correspondent process parameters.

Sample	Gas	Flow (SCCM)	Temperature (ºC)	Power (%)	Pressure (mbar)	Time (s)	HF dip	Position
RTH 1	5% H_2/Ar	40	1100	Varying	1.5	60	No	Up
RTH 2	5% H_2/Ar	1500	1100	Varying	12	60	No	Up
RTH 3	5% H_2/Ar	40	1200	Varying	1.5	20	No	Up
RTH 4	5% H_2/Ar	1500	1000	Varying	12	180	Yes	Up
RTA 10	Ar	40	1100	Varying	0.18	60	No	Up
RTA 11	Ar	1500	1100	Varying	12	60	No	Up
RTA 12	Ar	40	1200	Varying	0.18	20	No	Up

Up = Facing the chamber; **Up, covered** = facing the chamber, covered with an identical (in size) Si chip during the process; **Flipped** = Facing the carrier wafer; **HF dip** = 30s-HF chemical bath, immediately prior to processing.

As mentioned, due to some limitations of using Cr as a hard mask during the RTA processing, Al_2O_3 was the chosen material to replace it. Keeping the hard mask during RTP would allow observing if this alternative material would also be better suitable to withstand processing than Cr.

The initial approach compared the use of lower and higher pressure in Ar ambient and Ar with 5% H_2 ambient. Additionally, using identical flow and valve position, the minimum value for ambient pressure differs if using Ar or Ar with 5% H_2. Hence there cannot be a direct comparison as the conditions are not precisely similar. Nonetheless, as shown in Figure 7, some nuances are visible in the SEM analysis.

In another set of experiments, as shown in Figure 8, a higher temperature was used for a shorter period. Furthermore, the last pair of samples exemplify the effect of dipping the samples in the oxide etch chemical bath - containing 5% hydrogen fluoride (HF) - before RTH processing. The results are shown in Figure 9.
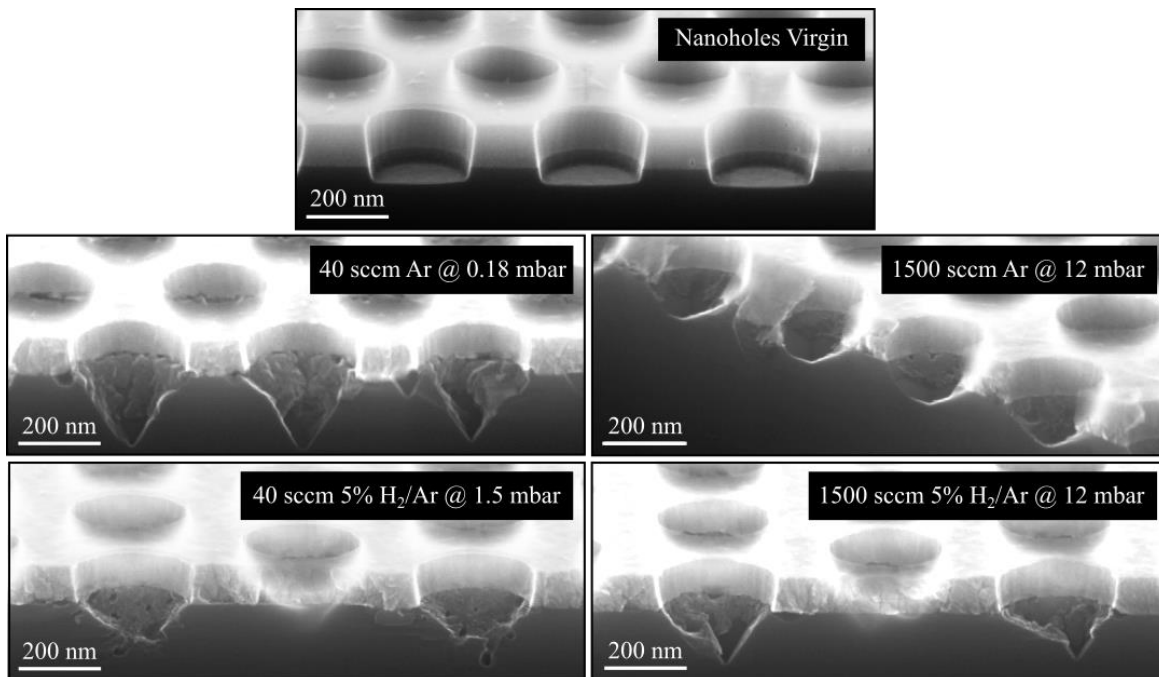
Figure 7 - Comparison of the effect of different pressure and ambient conditions on exposed Si, during RTA processing. Up-left) RTA 10; Down-left) RTA 11; Up-right) RTH 1; Down-left) RTH 2. Cross-section SEM images, 20° tilt, EHT 20 kV.
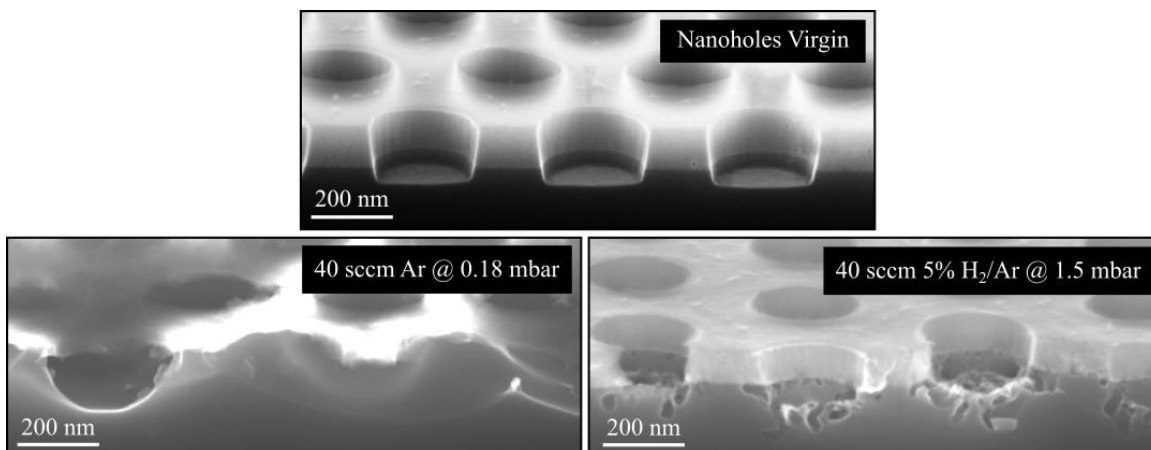
Figure 8 - Comparison of the effect of different ambient conditions on exposed Si, during RTA processing. RTA 12 on the left and RTH 3 on the right. Cross-section SEM images, 20° tilt, EHT 20 kV on the bottom-left image and EHT 5 kV on the bottom-right image.
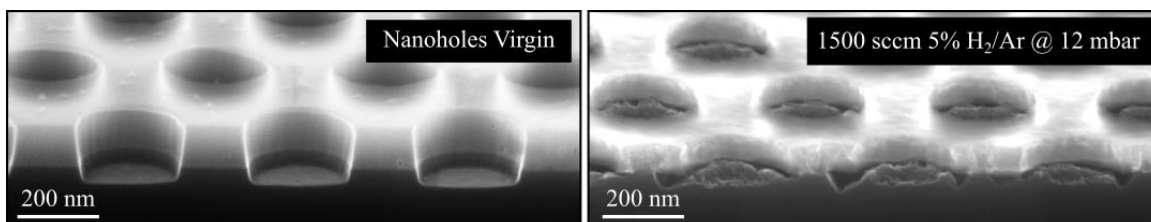
Figure 9 - Effect of HF dip on exposed Si before RTA processing (RTH 4 on the right). Cross-section SEM images, 20° tilt, EHT 20 kV.

In sum, thermal-induced defects were found, regardless of the combination of parameters used for RTH processing. If no other mechanism besides atom migration were present, then only some possible reshaping of the corners would be witnessed. However, the presence of this type of defect suggests the silicon is being etched. As such, the burning hypothesis was confirmed.

Moreover, no more silicon was found deposited on any of the quartz plates, after it has been thoroughly cleaned and the Si carrier wafers replaced by Si_3N_4-coated Si carrier wafers. This indicates that silicon sublimation and consequent deposition were present when using Si wafers – seemingly, the primary source of deposited silicon. Hence, it is safe to conclude that Si sublimation is also occurring from the samples, but in a smaller proportion, having a less meaningful impact on the quartz window.

In conclusion, it is confirmed that both phenomena occur for high and low temperatures as well as for high and low pressures/gas flows during RTH and Ar RTA processing. Nonetheless, using the **5% H₂/Ar mixture** as the process environment and **higher pressures combined with higher gas flows** is recommended to **prevent** surface attack. The process **temperature**, under temperature control, should **not surpass 1250 ºC**. Lastly, it is worth noticing that the **Al₂O₃ hard mask** emerges as an alternative **ideal masking material**, proven to be capable of sustaining RTP and suppressing the surface migration at the sample's surface.

2.3   Hydrogen/Argon RTA

Ar and 5% H₂/Ar rapid thermal annealing sequences were developed and studied. Type II samples were used and processed on top of Si_3N_4-coated Si carrier wafers, with no bonding required. The details for each experiment are presented in Table 4.

Table 4 – Hydrogen/argon rapid thermal annealing experiments and correspondent process parameters.

Sample	Gas	Flow (SCCM)	Temperature (ºC)	Power (%)	Pressure (mbar)	Time (s)	HF dip	Position
RTA 13	Ar	1500	1250	Varying	12	20	No	Up
RTA 14	Ar	1500	1250	Varying	12	40	No	Up
RTA 15	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	20	No	Up
RTA 16	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	20	No	Up
RTA 17	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	30	No	Up
RTA 18	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	30	No	Up
RTA 19	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	4	No	Up
RTA 20	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	8	No	Up
RTA 21	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	12	No	Up
RTA 22	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	16	No	Up
RTA 23	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	20	No	Up
RTA 24	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	20	No	Up
RTA 25	Ar + 5% H₂/Ar	2000 + 2000	1250	Varying	74	20	No	Up
RTA 26	Ar + 5% H₂/Ar	2000 + 2000	1100	Varying	74	20	No	Up
RTA 27	Ar + 5% H₂/Ar	2000 + 2000	1200	Varying	74	20	No	Up

Up = Facing the chamber; **Up, covered** = facing the chamber, covered with an identical (in size) Si chip during the process; **Flipped** = Facing the carrier wafer; **HF dip** = 30s-HF chemical bath, immediately prior to processing.

The initial experiment results (RTA 13 and RTA 14) are shown and compared in Figure 10.
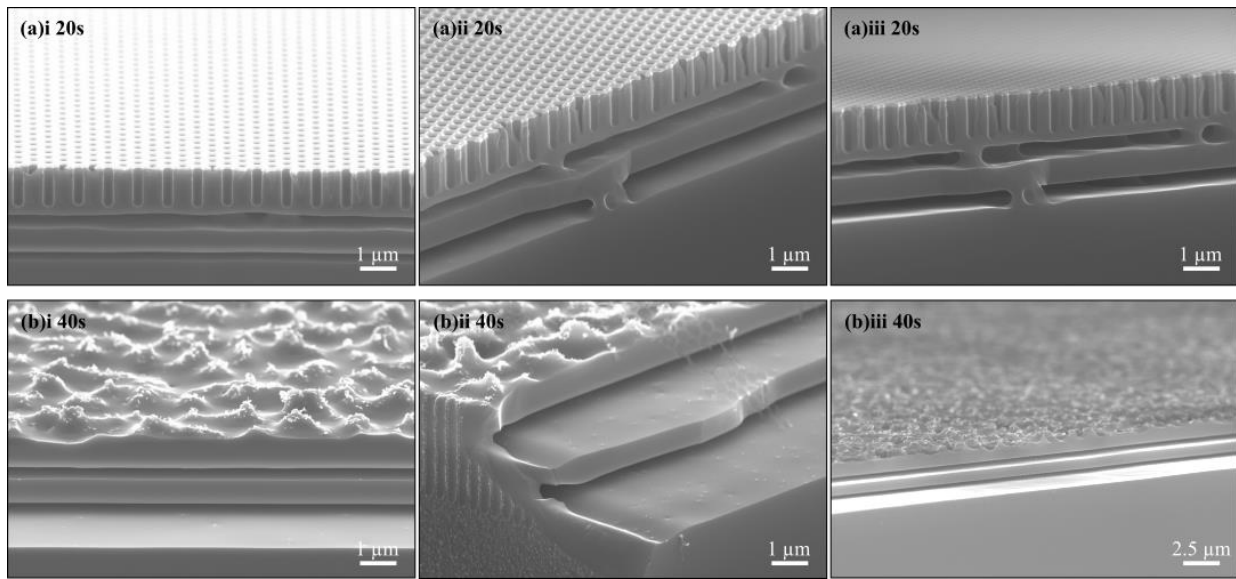
Figure 10 - Comparison of two consecutive experiments using different RTA times. Two images on the left represent an unprocessed nanoholes sample. (a)i and (a)ii correspond to the same sample (RTA 13), viewed from different angles. (b)i and (b)ii correspond to the same sample (RTA 14), viewed from different angles. Cross-section SEM images, 5° tilt on (a)ii and 20° tilt on the rest, EHT 5 kV on (a)i and (b)i and EHT 20 kV on the rest.

The gas flow and pressure were increased to preserve the hard mask and prevent the silicon's surface exposure, maintaining the temperature at 1250 ℃ and the process duration at 20 s (RTA 15). The result is shown in Figure 11. Furthermore, the experiment was repeated in a different sample (RTA 16) to assess the process reproducibility, maintaining the same RTA conditions and duration. The results are shown in Figure 12.
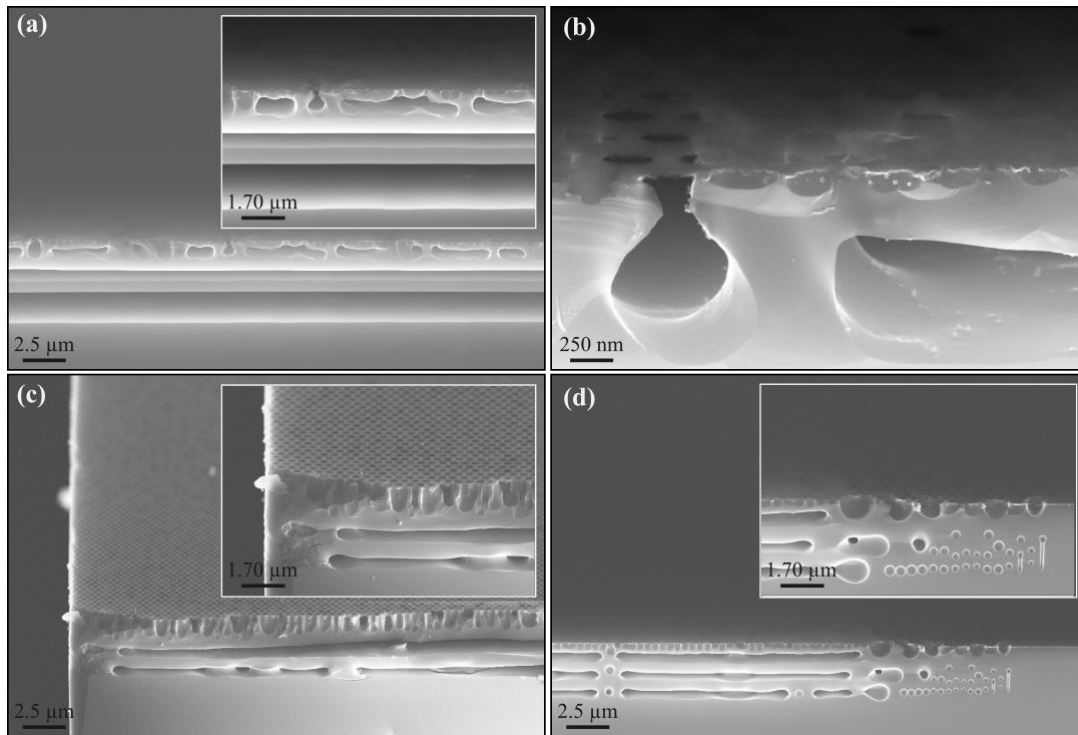
Figure 11 - Result no.1 from using a maximum pressure and gas flow RTA process (RTA 15). (a) and (b) are pictures from the centre of the sample. (c) and (d) are images taken at the end of the pattern on both sides of the sample. Cross-section SEM images, 20° tilt, EHT 20 kV.
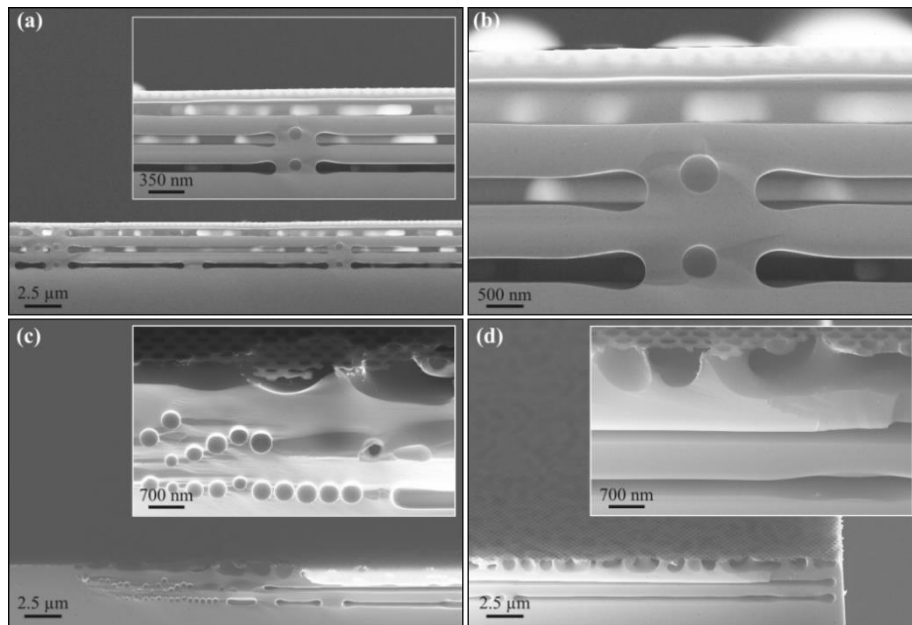
Figure 12 - Result no.2 from using a maximum pressure and gas flow RTA (RTA 16). (a) and (b) are pictures from the centre of the sample. (c) and (d) are pictures taken at the end of the pattern on both sides of the sample. Cross-section SEM images, EHT 20 kV, 0º tilt on (a) and (b), 20º tilt on (c) and (e).

Experiments 'RTA 17' and 'RTA 18' were executed to inquire if the tool's lack of reproducibility is also influenced by the position of the sample on top of the carrier wafer. With that purpose, two identical nanoholes-array chips were manually cleaved and broken in half, parallel to the <110> plane direction, and were annealed under similar RTA conditions. Both halves of the first chip were processed together, and then the remaining two halves. The results are shown and compared in Figure 13.
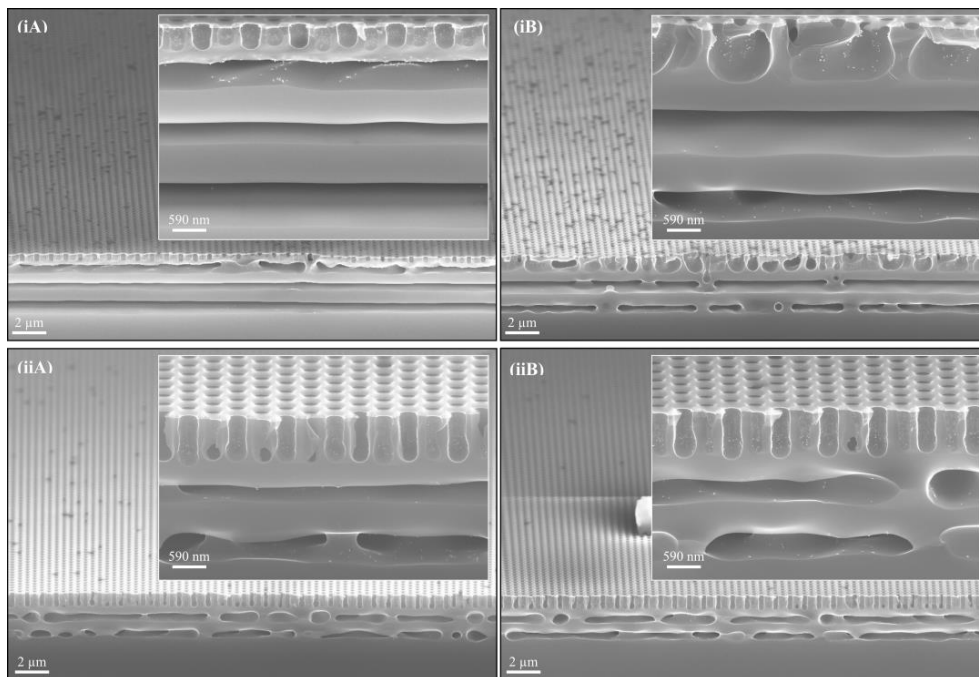
Figure 13 - Results of RTA processing using 2 pairs of half-samples, each pair processed together, placed next to each other on top of the Si_3N_4 carrier wafer. (iA) and (iB) are halves of the same chip (RTA 17), as well as (iiA) and (iiB) (RTA 18). The process parameters were 30 s, 1200 ºC, 74 mbar, 2000 SCCM Ar and 2000 SCCM 5% H_2/Ar. Cross-section SEM images, 20º tilt, EHT 20 kV.

Yet another approach was taken, using relatively similar type II samples. Compared with the other set of samples used in this study, they only differ in depth and etching profile – these are 4 µm deep and present a slightly positive profile (Figure S2). Nonetheless, a less straight profile is interesting to test the already working RTA recipes. Accordingly, this new set of samples was annealed using the 1250 ºC RTA process, with maximum gas flow and high pressure, for different periods. As such, a visual temporal evolution of the buried features formation process was attempted, revealed in Figure 14, corresponding to experiments 'RTA 19' to 'RTA 22'.
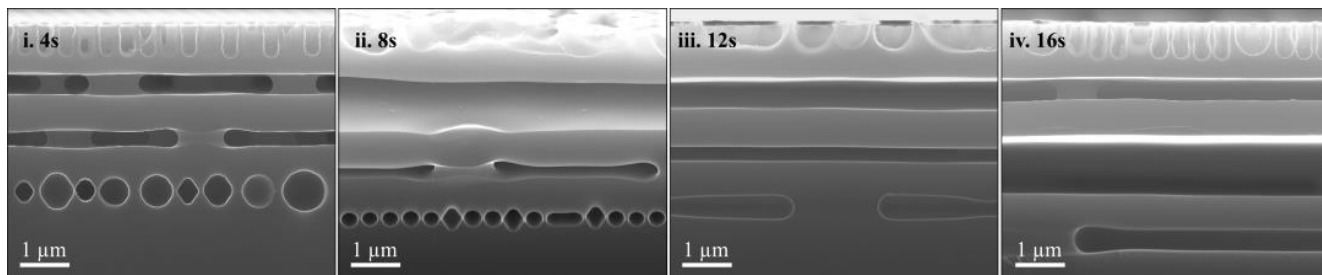
Figure 14 - Comparison between different consecutive experiments using different RTA processing times (RTA 19 - RTA 22). Cross-section SEM images, 0º tilt on (i), (iii) and (iv), 20º tilt on (ii), EHT 20 kV.

Moreover, the process reproducibility was also studied (RTA 23 to RTA 25) using the new set of type II samples (4µm-deep nanoholes, slightly positive-tapered). The results are visible in Figure 15.
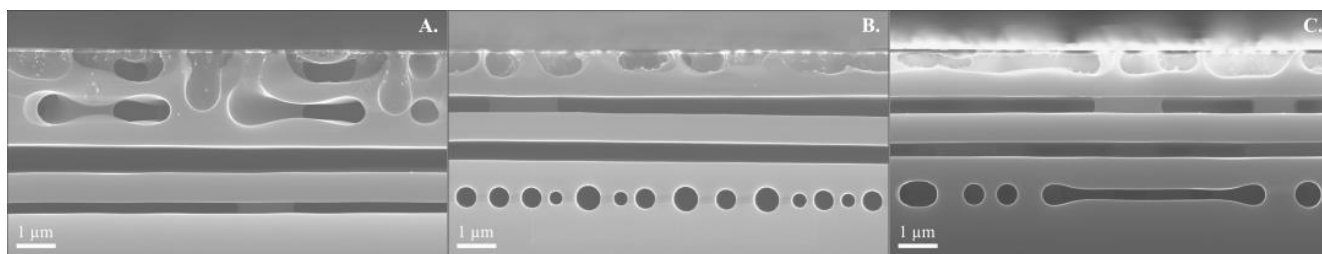
Figure 15 - Comparison between three consecutive experiments undergoing an identical RTA process (RTA 23 – RTA 25). Cross-section SEM images, 0º tilt, EHT 20 kV.

For the last set of experiments (RTA 26 and RTA 27), a different perspective was studied – the effect of using different temperatures during the RTA process.
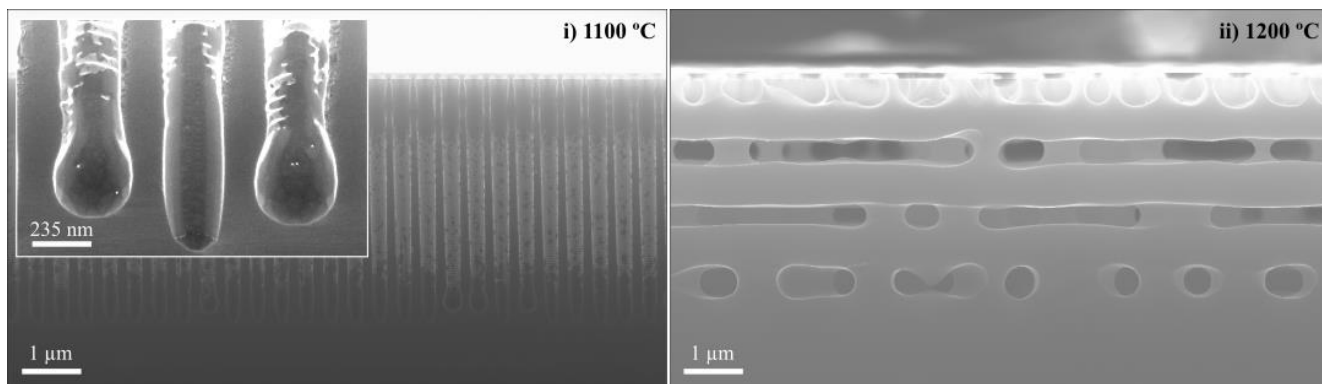
Figure 16 – Comparison between two consecutive experiments using different RTA temperatures: i) RTA 26 and ii) RTA 27. Cross-section SEM images, 0º tilt, EHT 20 kV. In the magnified picture, in the top-left, there's a 20º tilt.

Overall, the results have confirmed the non-reproducibility of the RTA process, even though they were carried out under sublimation and etching-minimizing conditions. Nonetheless, this study has proved that the formation of ESS is not exclusively correlated with H_2-ambient RTA processing. On the contrary, differently shaped ESS were obtained using a mixture of both Ar and H_2, with only 5% H_2, using distinct process conditions. Additionally, it allowed a better comprehension of the early stages of the buried channel/cavity formation, indicating that the appearance of spherical ESSs starts at the bottom of the inlets.

Moreover, another possible cause was considered to explain the tool's inability to produce identical results. Besides sublimation and burning - phenomena that have been established are occurring during the annealing sequences - another issue was raised when using high flows of the 5% H_2/Ar mixture. The tool is obliged to perform a post-cleaning process by flushing N_2 into the chamber, whereas the atmospheric pressure is reached in just a few seconds. Thus, there is a possibility that this rapid change in pressure and gas flow is causing one of the quartz pins supporting the carrier wafer to be expelled from its place, as it is just docked in another quartz piece. Hence, the unbalanced carrier wafer leads the samples resting on top to slide and sometimes even fall off into the chamber. During this set of experiments, it was noticed that several samples, after being out of the chamber (in the loadlock), either were rotated, rotated in a different position or were not there. In case of falling, the samples were later found and retrieved from inside the chamber, along with the expelled pin. As a result, opening the chamber several times caused its pre-conditioning to be changed over time, which might have led to a deterioration of process reproducibility. Similar process disturbance may also be the case when the samples would just slide or rotate, even without falling. In an attempt to fix this recurring issue, a soft-start valve was installed to prevent the pressure-rising from being so abrupt and minimize the number of samples lost inside the chamber. Ultimately, the number of times the chamber had to be disturbed would also decrease. Nonetheless, the cause behind **the falling-pins issue is yet to be deepened**, as the soft-start valve installation proved to be insufficient in solving the problem. Equally important, it would be of interest to guarantee the process gases' purity and minimize the quantity of oxygen inside the chamber by **adding a gas purifier**. As such, the silicon surface attack by reaction with oxygen could be avoided.

In general, for hydrogen/argon RTA sequences, from the process parameters perspective, it is recommended that the temperature does **not surpass 1250 ºC.** In addition, the **pressure** and **gas flow** should be set to **high values** - sublimation/burning minimizing conditions - **not higher than 2000 SCCM** for each gas line and up to **74 mbar.** Higher pressures (**83 mbar**) were safely tested, inducing no damage to the tool.

2.4   Clean BSi

Ar and 5% H_2/Ar rapid thermal annealing recipes were developed and studied in order to be used as BSi removal sequences. Type III samples were used and processed on top of Si_3N_4-coated Si carrier wafers, with no bonding required. A type IV sample was also used. The details for each experiment are presented in Table 5.

The present study was pursued as the tool was considered an available approach to eliminate BSi from carrier wafers, already used in the DRIE tool a substantial number of times. Furthermore, the goal was to recycle them as an alternative to using new ones. Figure 17 shows the visual effect of this 'cleaning' process (RTA 28). As a result, more experiments were carried out to understand how to induce BSi smoothing and the factors affecting it.

As initial approach, the effect of temperature was investigated (RTA 29-32). The results are shown in Figure 18.

Table 5 – Rapid thermal annealing experiments applied to BSi removal and correspondent process parameters.

Sample	Gas	Flow (SCCM)	Temperature (ºC)	Power (%)	Pressure (mbar)	Time (s)	Sample type	Position
RTA 28	Ar	40	1283	70	0.18	8	IV	-
RTA 29	Ar	40	1000	Varying	0.18	1	III	Up
RTA 30	Ar	40	1100	Varying	0.18	1	III	Up
RTA 31	Ar	40	1200	Varying	0.18	1	III	Up
RTA 32	Ar	40	1309	70	0.18	1	III	Up
RTA 33	Ar	40	1000	Varying	0.18	4	III	Up
RTA 34	Ar	40	1000	Varying	0.18	8	III	Up
RTA 35	Ar	40	1000	Varying	0.18	12	III	Up
RTA 36	Ar	40	1000	Varying	0.18	16	III	Up
RTA 37	Ar	40	1000	Varying	0.18	20	III	Up
RTA 38	Ar	40	1000	Varying	0.18	30	III	Up
RTA 39	Ar	40	1000	Varying	0.18	60	III	Up
RTA 40	Ar	40	1000	Varying	0.18	10	III	Up
RTA 41	Ar	2000	1000	Varying	43	10	III	Up
RTA 42	Ar	40	1200	Varying	0.18	1	III	Up
RTA 43	Ar	2000	1200	Varying	43	1	III	Up
RTA 44	5% H_2/Ar	40	1000	Varying	1.5	10	III	Up

Up = Facing the chamber; **Up, covered** = facing the chamber, covered with an identical (in size) Si chip during the process; **Flipped** = Facing the carrier wafer; **HF dip** = 30s-HF chemical bath, immediately prior to processing.
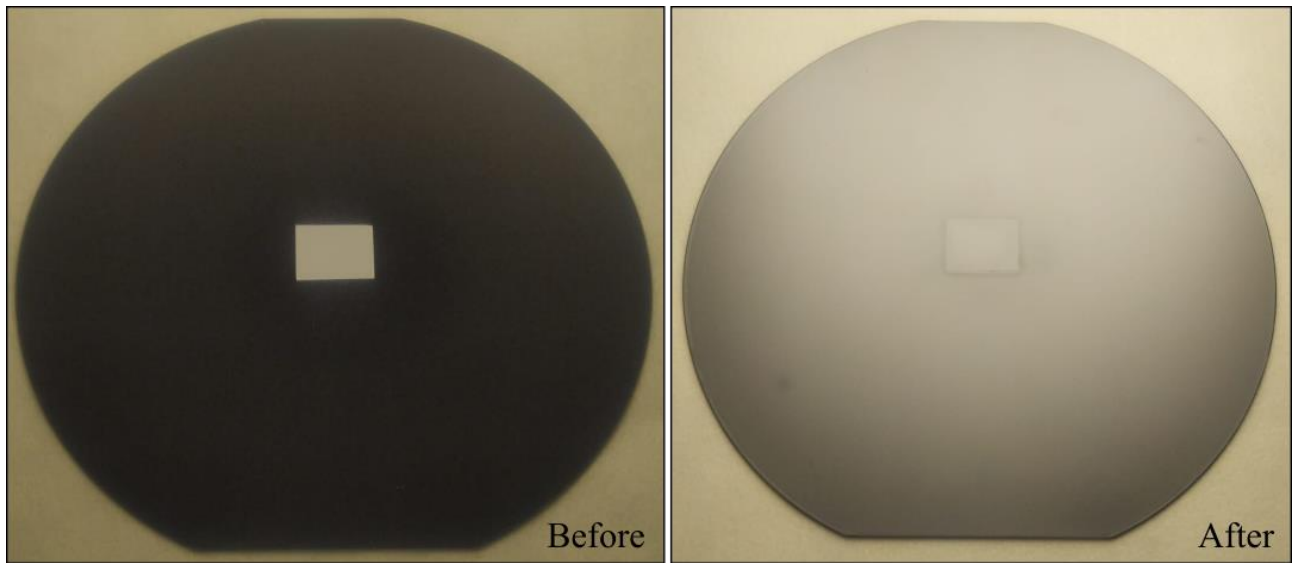
Figure 17 - BSi wafer before and after undergoing an 8s-RTA process showing the effect RTA has on BSi removal (RTA 28). Digital camera images, 150 mm Si wafer, unpolished side up.
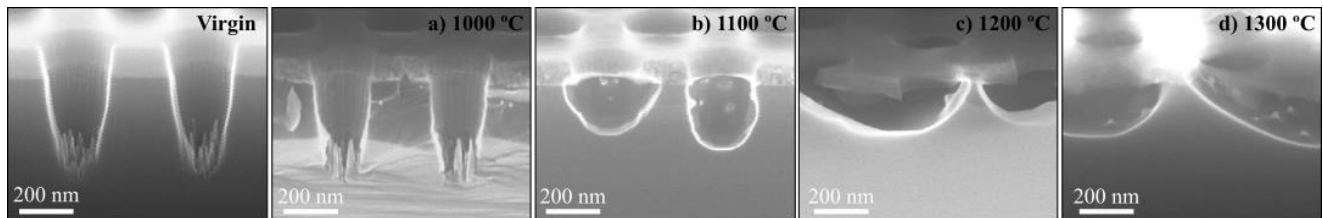
Figure 18 - Effect of temperature on the BSi removal process achieved by RTA (RTA 29 – RTA 32). Cross-section SEM images, 20º tilt and EHT 20 kV.

Furthermore, the effect of time was studied (RTA 33 – RTA 29), as shown in Figure 19.
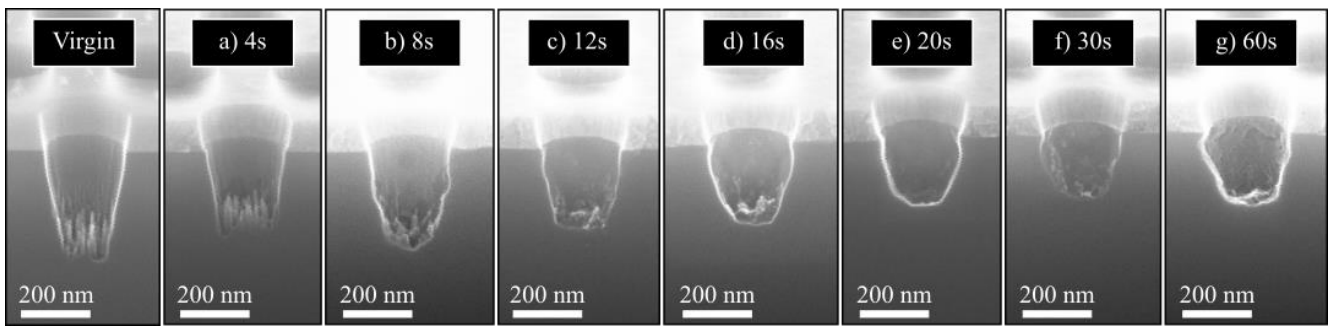
Figure 19 - Effect time has on the BSi removal process (RTA 33 – RTA 29). The process parameters were 1000 ºC, 0.18 mbar and 40 SCCM Ar. Cross-section SEM images, 20º tilt and EHT 20 kV.

Lastly, the influence of flow and pressure *vs.* temperature (RTA 40 – RTA 43) and the presence of hydrogen (RTA 44) was explored. The results are shown in Figure 20 and Figure 21, respectively.
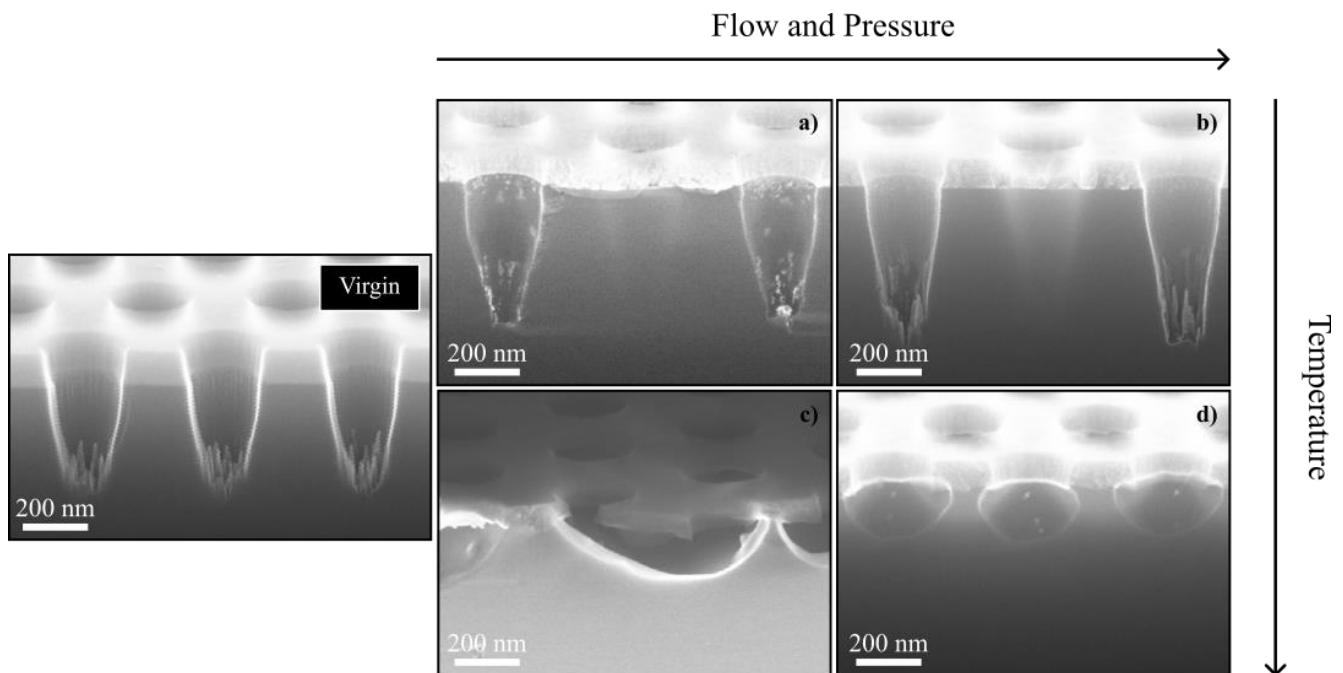
Figure 20 - Flow and Pressure vs Temperature effect on the BSi removal process. a) RTA 40; b) RTA 41; c) RTA 42; d) RTA 43. Cross-section SEM images, 20º tilt and EHT 20 kV.
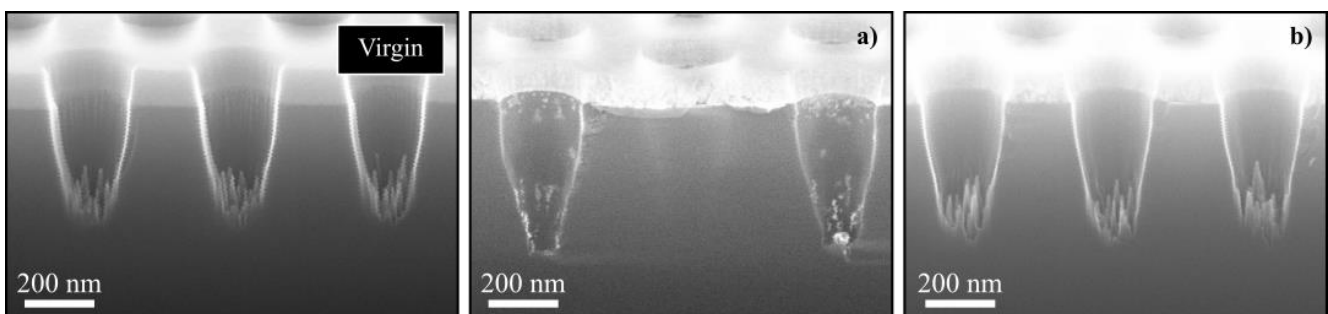
Figure 21 - Effect the process gas has on the BSi removal process. a) RTA 40; b) RTA 44. Cross-section SEM images, 20º tilt, EHT 20 kV.

Taking advantage of the smoothing caused by atom migration during RTA processes, this combination of experiments aimed to prove that BSi removal could be achieved using the same tool. Accordingly, the elimination of BSi, previously grown using the CORE process in Si wafers and at the bottom of nanoinlets, was successfully achieved. The effect of temperature, time, pressure/flow combination and process gas were investigated as improving factors for the RTA process involved. However, neither of the used combinations of parameters was ideal for removing the BSi while preserving the nanoinlet shape and enhancing the surface smoothness. As such, **further work is required to establish the ideal process window**. Nevertheless, the results from this study were consistent with those from the other set of testes and sustained every former conclusion.

2.5 RTO

This chapter is dedicated to analyzing and discussing the results achieved using one of the other features of the rapid thermal processor tool – RTO. This study aimed to reflect the effects of rapid thermal oxidation on HAR Si features. Thereupon, it was necessary to establish a process window and ensure the process was reproducible within those parameters. Hence, the study was initiated by testing the reproducibility and stability of a programmed RTO recipe using type V samples. Additionally, type II samples were used for the HAR structures testing. These were processed on top of silicon nitride (Si_3N_4) coated silicon carrier wafers, without any bonding. The details of each experiment are listed in Table 6.

Table 6 - Rapid thermal oxidation experiments and correspondent process parameters.

| Sample	Gas	Flow (SCCM)	Temperature (ºC)	Power (%)	Pressure (mbar)	Time (s)	Sample type	Rounds
RTO 1	O_2	1500	1200	Varying	12	0.1	V	3
RTO 2	O_2	1500	1200	Varying	12	60	V	3
RTO 3	O_2	1500	1200	Varying	12	120	V	3
RTO 4	O_2	1500	1200	Varying	12	180	V	3
RTO 5	O_2	1500	1200	Varying	12	300	V	3
RTO 6	O_2	1500	1200	Varying	12	600	V	2
RTO 7	O_2	1500	1200	Varying	12	900	V	2
RTO 8	O_2	1500	1200	Varying	12	1200	V	2
RTO 9	O_2	1500	1200	Varying	12	1500	V	2
RTO 10	O_2	1500	1200	Varying	12	1800	V	2
RTO 11	O_2	1500	1200	Varying	12	2100	V	2
RTO 12	O_2	1500	1200	Varying	12	2400	V	2
RTO 13	O_2	1500	1200	Varying	12	2400	II	-

The dataset for each RTO round (Table 7) was plotted together and can be found in Figure 22 (RTO 1 – RTO 12). For each round, each point represents an ellipsometry measurement, with corresponding error bars (based on the mean squared error (MSE) for each). It is essential to mention that the RTO sequence is programmed to include an initial 10s-interval to stabilize the temperature inside the chamber as well as pressure and gas flow. However, this interval is not included in the designated RTO process time; the RTO process is only considered to have begun after this period. There might be SiO_2 growth during the stabilization period as the temperature is already being increased. Hence, the initial thickness cannot be considered zero. To determine the initial oxide thickness before RTO processing, i.e., after the 10s-period, the RTO process time was fixed to 0 s (0.1 s, as the machine does not allow to insert 0 s as the step time).

Table 7 - Average thickness ellipsometry measurements and correspondent MSE, for each oxidation time and round (RTO 1 – RTO 12). The third-round dataset is not completed as one of the quartz-window broke mid-process.

Oxidation time	Round 1		Round 2		Round 3	
	Measurement (nm)	MSE	Measurement (nm)	MSE	Measurement (nm)	MSE
0.1 s (0 s)	1.30	1.550	1.36	1.407	1.41	1.385
60 s	2.84	1.608	2.97	1.389	2.90	1.394
2 min	3.82	1.605	3.80	1.411	3.83	1.393
3 min	4.48	1.616	4.54	1.383	4.55	1.383
5 min	5.75	2.049	5.60	1.627	5.68	1.621
10 min	8.12	2.189	7.92	1.681	-	-
15 min	11.71	5.209	10.86	1.401	-	-
20 min	13.00	4.851	12.39	1.507	-	-
25 min	13.62	5.188	13.53	1.379	-	-
30 min	15.31	5.382	14.80	1.410	-	-
35 min	15.93	1.393	15.98	1.376	-	-
40 min	16.81	1.810	16.84	1.226	-	-
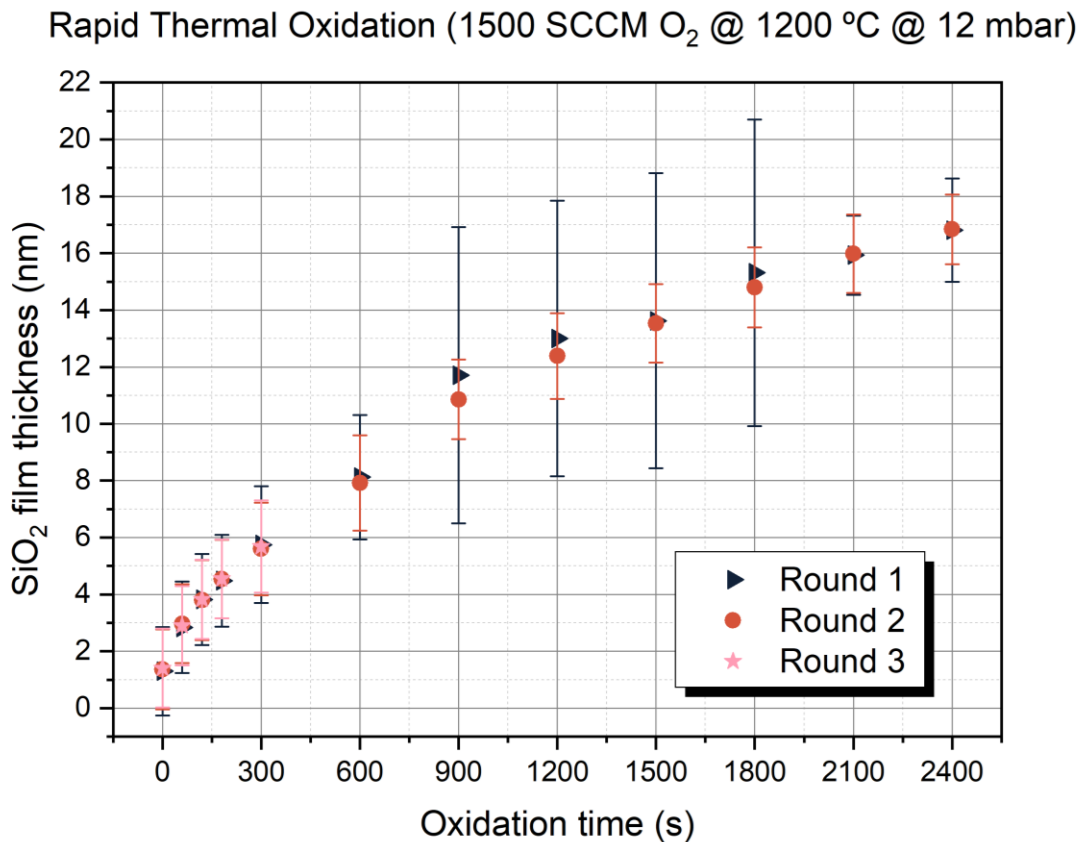
Figure 22 - Graphic representation of the correlation between SiO_2 thin film growth and oxidation time. The third-round dataset (pink stars) is not completed as one of the quartz-window broke mid-process.

Moreover, the characterization performed by ellipsometry allowed an analysis from a film uniformity perspective. This analysis was as necessary as the previous one since it can provide information about heat distribution across the whole wafer used during the RTO process. Figure 23 shows different colour maps for each RTO process time.

The maps were achieved by using the average film thickness on nine distinct points of the wafers, considering the three rounds of experiments. The dark-lined circle represents the wafer area.
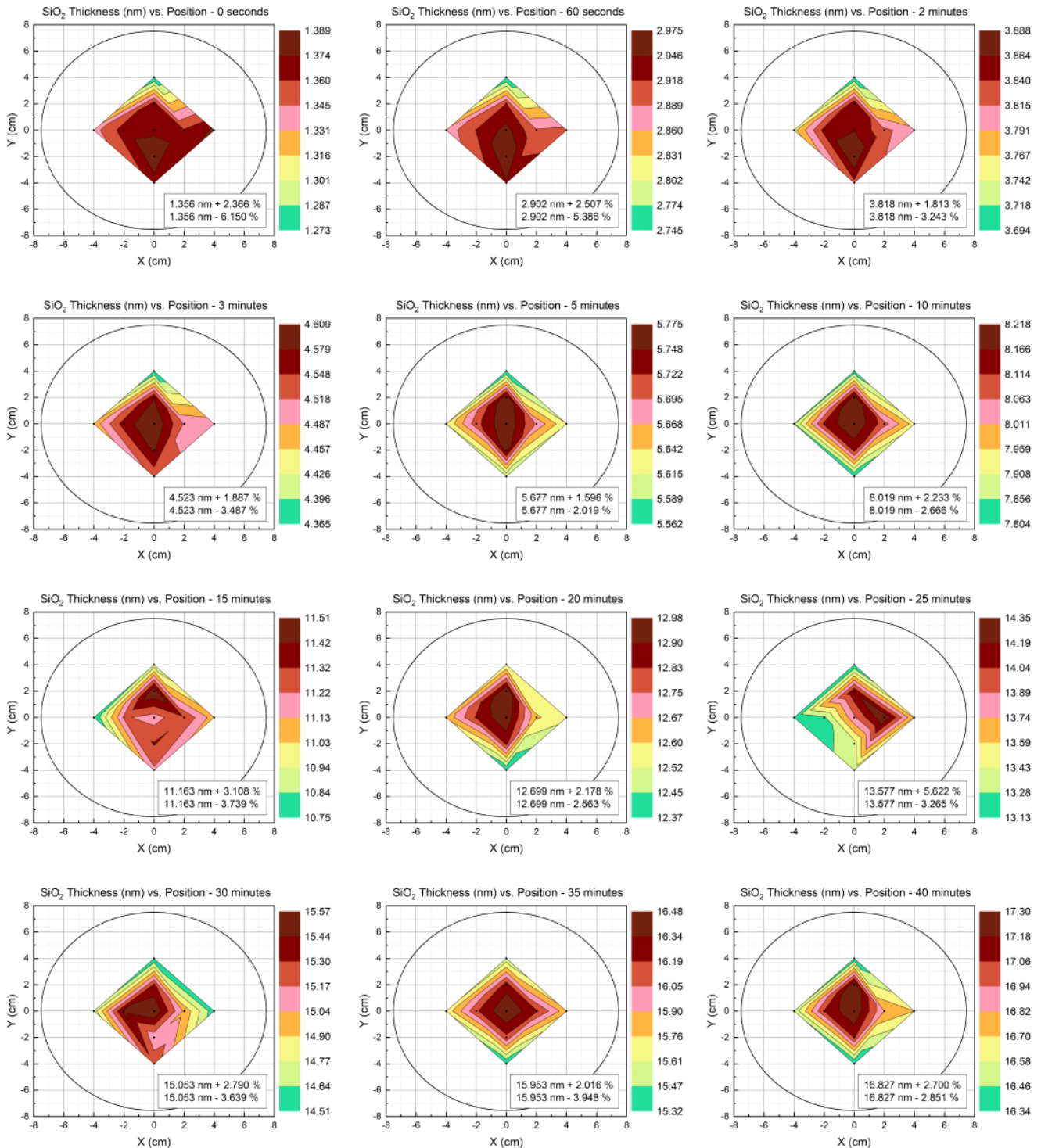
Figure 23 - Graphic representations of the grown SiO_2 thin film thickness vs position in the wafer for different RTO process times. It is also indicated the thickness variation (in percentage) when compared with the average oxide thickness across the wafer.

Moreover, a 40min-RTO process was performed as it corresponds to a higher oxide thickness growth, being the easiest one to capture using the SEM tool. The results are shown in Figure 24.
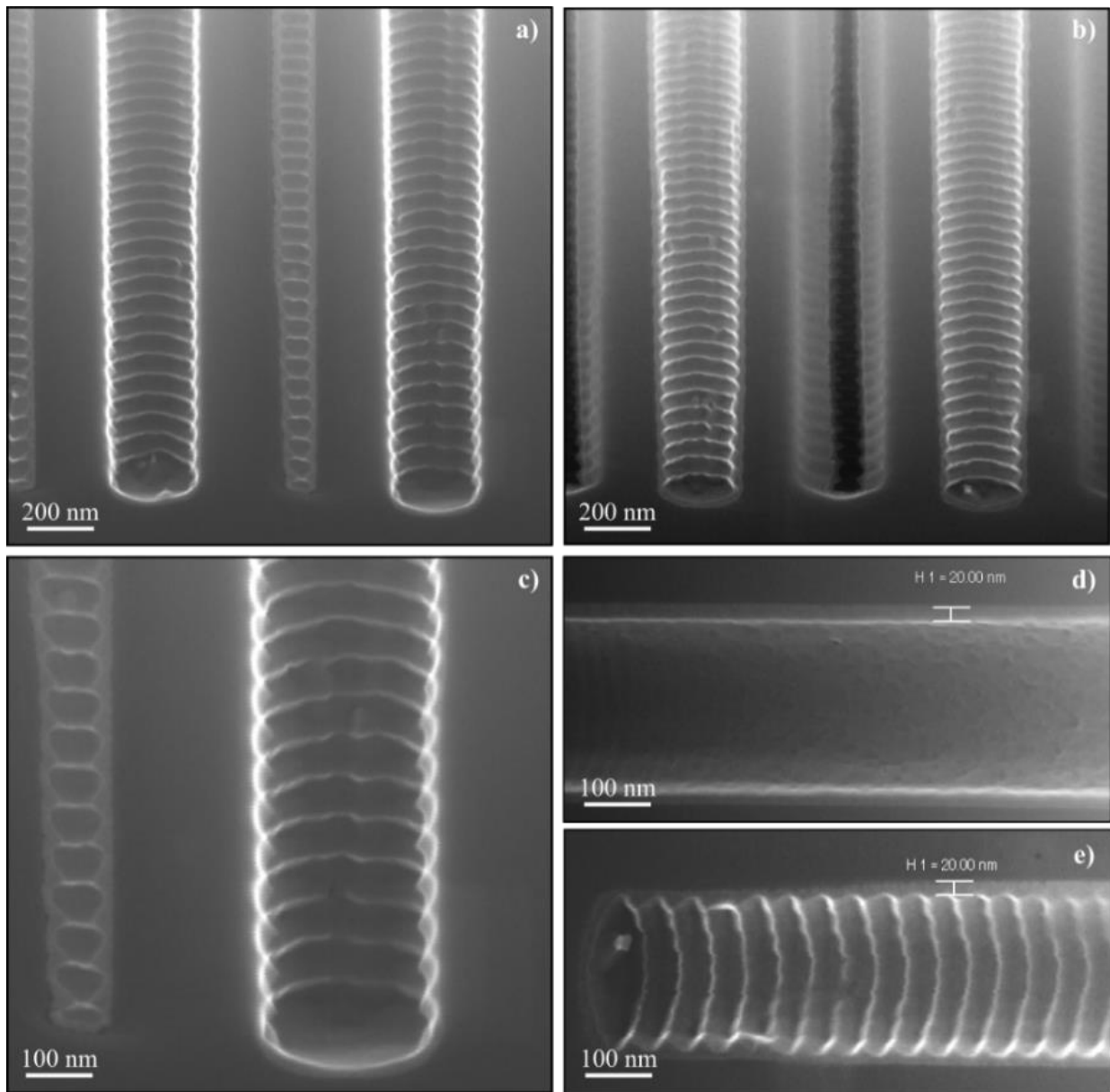
Figure 24 - Nanoholes sample a), c) before and b), d), e) after a 40min-RTO process (RTO 13). Pictures d) and e) were rotated during the characterization due to some existing vibrations preventing a good resolution in the vertical position. The thermal oxide thickness was measured in two places (d)top and e)bottom) of the inlet using the SEM tool. Cross-section SEM images, 20º tilt and EHT 20 kV.

In conclusion, RTO processing was regarded as a relatively stable and repeatable process. For Si (100) surfaces and Si (110) surfaces, SiO$_2$ thin films could be grown with only minor uniformity issues, below 17 nm and 20 nm, respectively. Nonetheless, more experiments carried out under different conditions – such as temperature, pressure, oxygen flow and even shorter oxidation periods - would be helpful to study further the RTO process and consequently model the experimental data. The uniformity issues could be addressed by exploring the lamp compensation capabilities.

It is also worthwhile mentioning, The top quartz plate was replaced twice, as two of them broke mid-process during 10min-RTO sequences. Thus, RTO should **not be performed** for more than **5 min**, at such high temperature.

2.6   RTV

A rapid thermal processing sequence under high vacuum was also developed. For this set of experiments, type II samples (before undergoing the final Si etch step) were used and processed on top of Si_3N_4-coated silicon carrier wafers, without any bonding. The experimental details are presented in Table 8.

Table 8 – Rapid thermal processing under high vacuum experiments and correspondent process parameters.

Sample	Gas	Flow (SCCM)	Temperature (ºC)	Power (%)	Pressure (mbar)	Time (s)	HF dip	Position
RTV 1	No	0	1100	Varying	$< 6 \times 10^{-6}$	60	No	Up
RTV 2	No	0	1100	Varying	$< 8 \times 10^{-6}$	300	No	Up

As shown in Figure 25 and Figure 26, two different experiments (RTV 1 and RTV 2) were attempted, using identical conditions except for time.
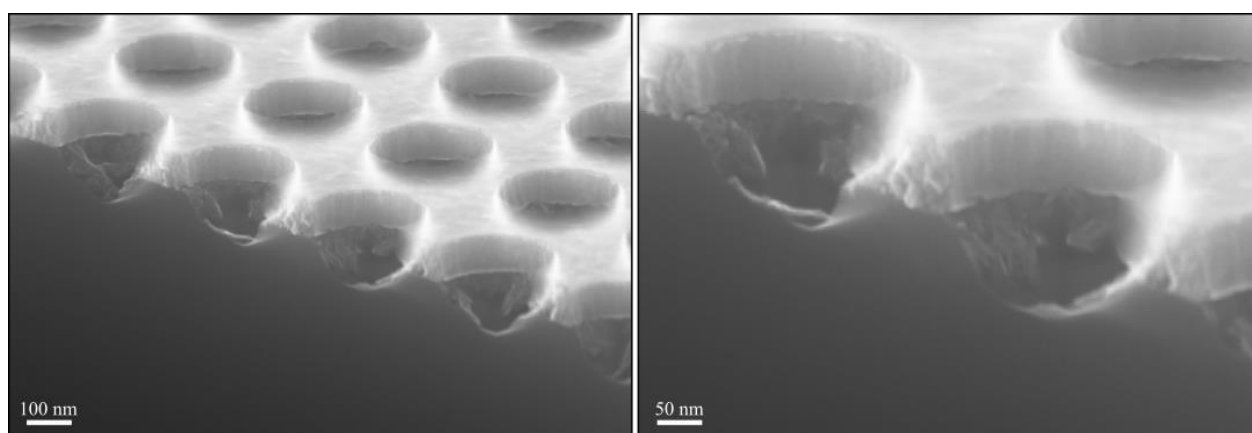
Figure 25 – Effects on silicon after a 1min-RTV process (RTV 1). Cross-section SEM images, 20º tilt and EHT 20 kV.
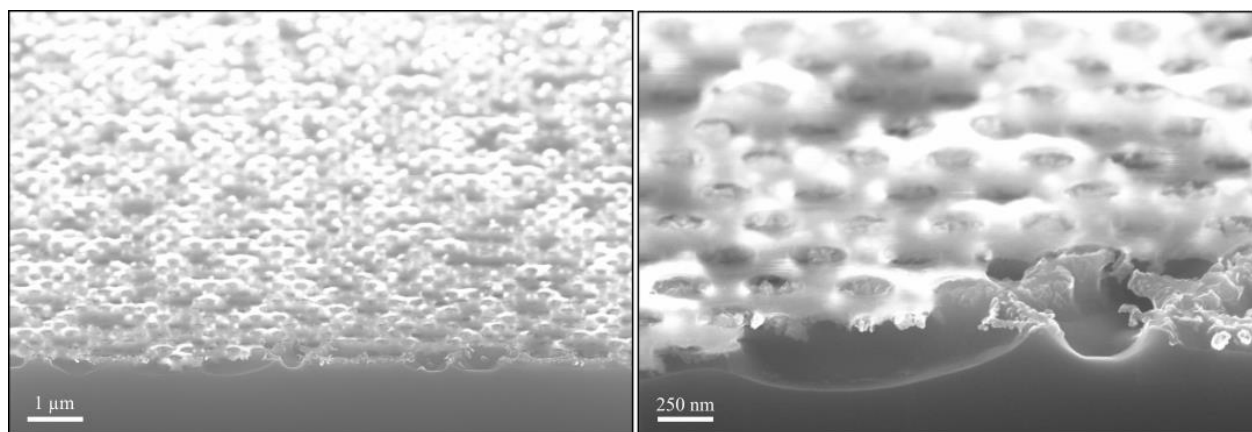
Figure 26 - Effects on silicon after a 5min-RTV process (RTV 2). Cross-section SEM images, 20º tilt and EHT 20 kV.

The effects witnessed using RTV sequences are very similar to the ones obtained while using RTH sequences. Therefore, it is possible to assume there are sublimation and burning mechanisms present during RTV, even though no process gas was inserted inside the chamber. As such, it sustains the hypothesis that the chamber is not oxygen-free during processing. As already stated, a gas purifier could be the solution to solving this recurring issue. Overall, it is required to further test these recipes to obtain more information about their effects on HAR structures and recommended process windows.

2.7 Tool calibration

A tool calibration sequence was developed in order to ensure process temperature reliability. It is performed prior and after the tool is used for processing samples. For that reason, a Si_3N_4-coated Si wafer (double-side polished) was selected and reserved as a calibration wafer. All calibrations were performed on this wafer. The recipe parameters are observed in Table 9.

Between sequences, if the temperature does not present significant changes, then the machine is calibrated. Any significant temperature change (50 °C or higher) between calibrations might indicate Si accumulation on the quartz plates. Thus, a calibration sequence should also be used after BSi-removal sequences on full wafers, in which Si sublimation and consequently deposition on the top quartz plate are likely to occur, with a major impact.

Table 9 – Calibration sequence process parameters.

	Gas	Flow (SCCM)	Power (%)	Pressure (mbar)	Time (s)	Average Temperature (ºC)
Calibration recipe	Ar	40	70	0.18	8	≈ 1288

Throughout the experimental work, every calibration temperature was registered, as presented in Table S1. Figure 27 shows the dataset plotted together, as well as the average value for the calibration temperature.
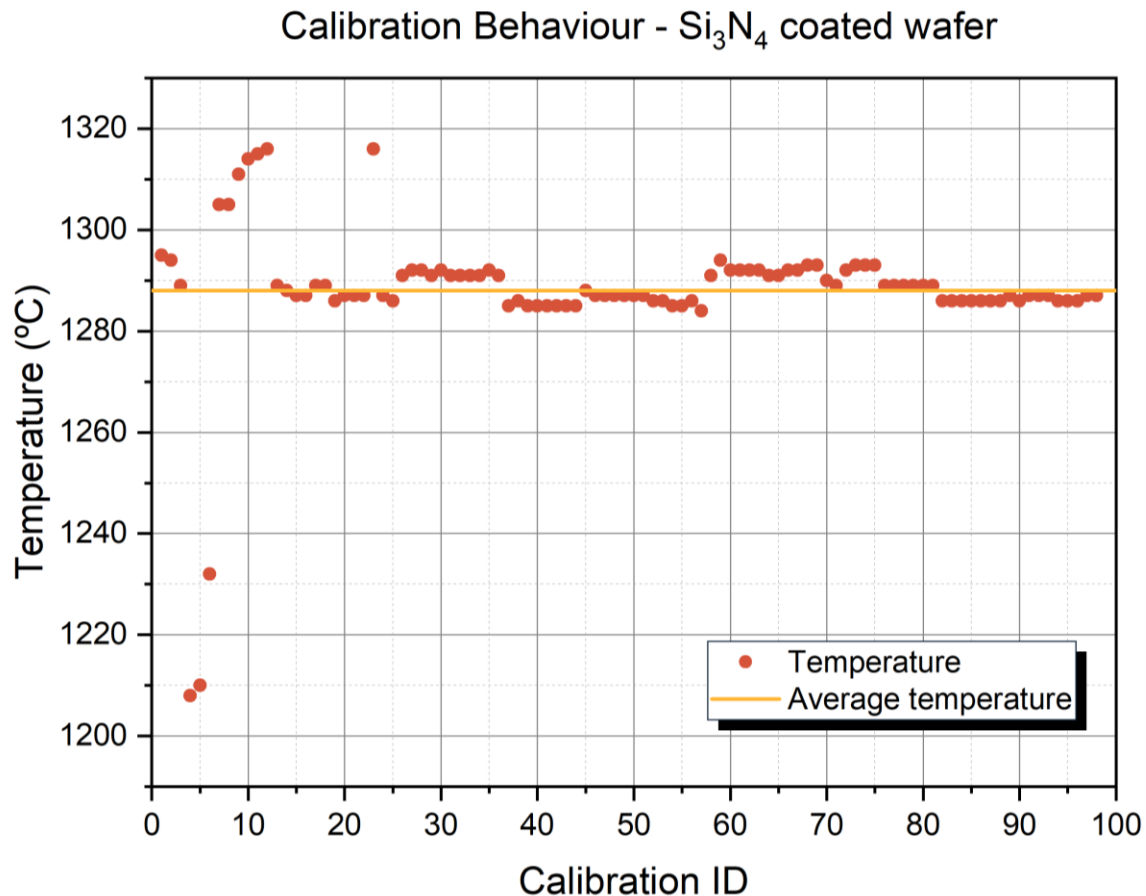

Figure 27 – Calibration sequence behaviour, throughout the experimental work, when using the Si_3N_4 coated Si wafers (calibration wafer).

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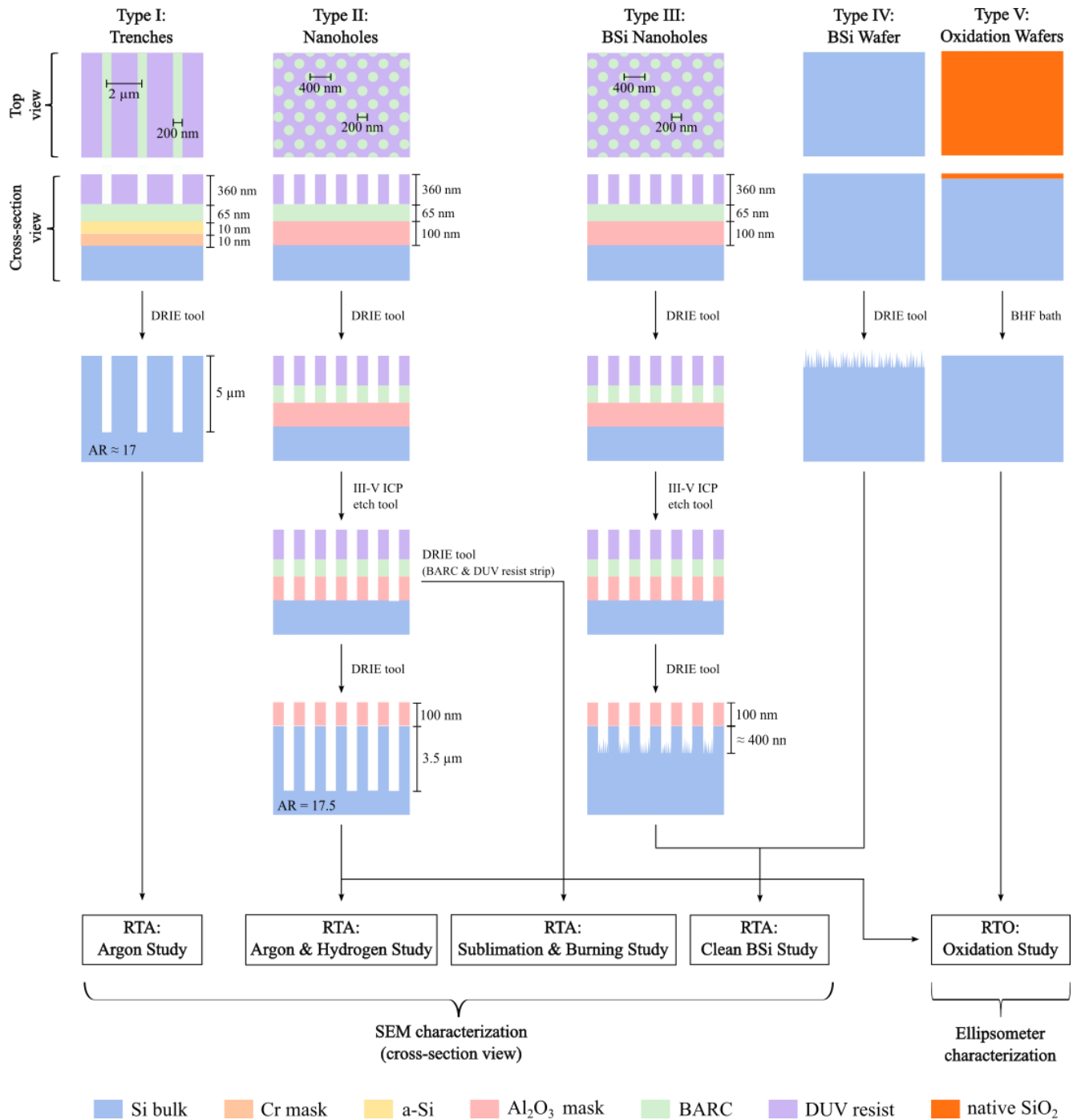
A   Supplementary Figures

Figure S1 - Schematic representation of the fabrication process flow for each type of sample used during the experimental work. The drawings are not to scale.
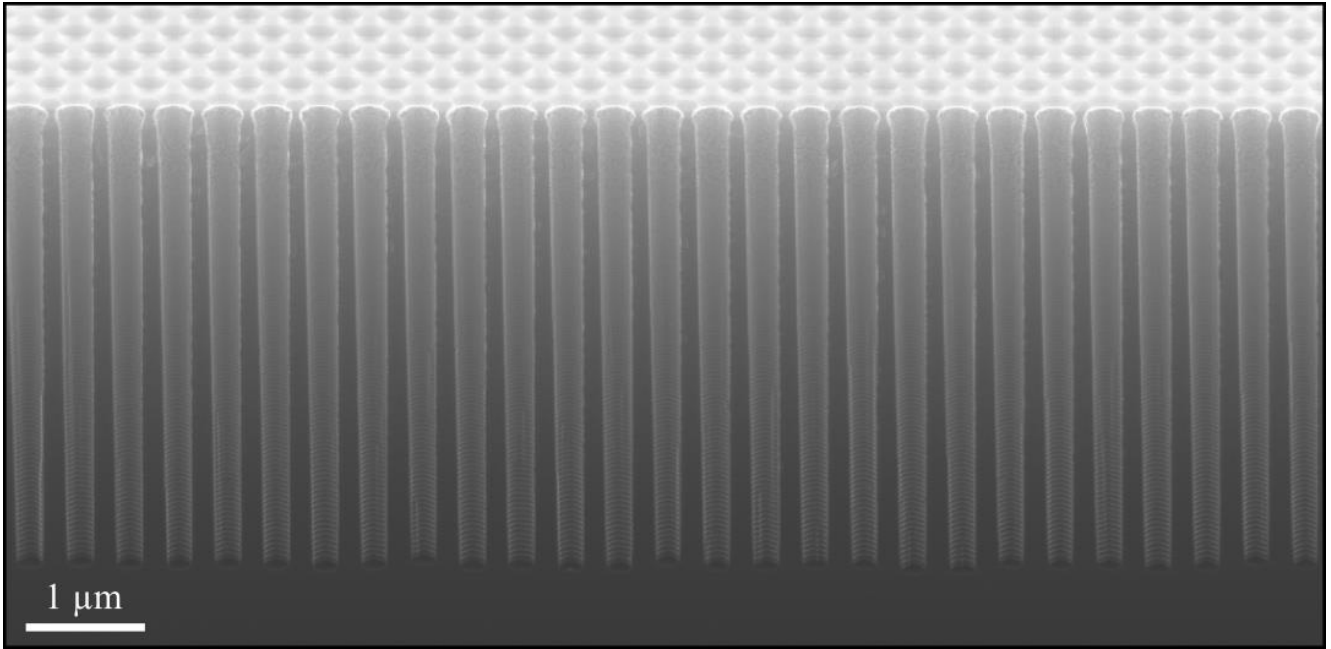
Figure S2 - Nanoholes sample from a new batch after re-conditioning the DRIE tool. The holes are 4 µm deep and have a 200nm-diameter and 400nm-pitch. Cross-section SEM images, 20° tilt, EHT 20 kV.

B Supplementary Tables

Table S1 – List of every calibration sequence performed and corresponding measured temperatures (maximum).

Calibration ID	Temp. (ºC)	Calibration ID	Temp. (ºC)	Calibration ID	Temp. (ºC)	Calibration ID	Temp. (ºC)
001	1295	026	1291	051	1287	076	1289
002	1294	027	1292	052	1286	077	1289
003	1289	028	1292	053	1286	078	1289
004	1208	029	1291	054	1285	079	1289
005	1210	030	1292	055	1285	080	1289
006	1232	031	1291	056	1286	081	1289
007	1305	032	1291	057	1284	082	1286
008	1305	033	1291	058	1291	083	1286
009	1311	034	1291	059	1294	084	1286
010	1314	035	1292	060	1292	085	1286
011	1315	036	1291	061	1292	086	1286
012	1316	037	1285	062	1292	087	1286
013	1289	038	1286	063	1292	088	1286
014	1288	039	1285	064	1291	089	1287
015	1287	040	1285	065	1291	090	1286
016	1287	041	1285	066	1292	091	1287
017	1289	042	1285	067	1292	092	1287
018	1289	043	1285	068	1293	093	1287
019	1286	044	1285	069	1293	094	1286
020	1287	045	1288	070	1290	095	1286
021	1287	046	1287	071	1289	096	1286
022	1287	047	1287	072	1292	097	1287
023	1316	048	1287	073	1293	098	1287
024	1287	049	1287	074	1293	-	-
025	1286	050	1287	075	1293	-	-