Smooth nitride etching with Cr hardmask

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Intro

This is a brief note describing process development of two etching recipes at DTU Nanolab, one for etching silicon nitride with smooth sidewalls with a Cr hard mask, and the other for etching the Cr mask itself. The reason for the effort is to make photonic structures in stoichiometric Si_3N_4 with aspect ratio around one and very low scattering loss, which requires the lowest possible sidewall roughness. State-of-the-art fabrication of low-loss nitride waveguides use a dry-etching recipe with oxygen to prevent carbon polymers from forming on the sidewall. However, that means the usual resist mask will be attacked, prompting the use of hard masks – usually Cr or SiO_2. We have focused on Cr.

Cr etching

Development was done on the *ICP metal* etcher. We used mostly one or a few smaller chips (1x1 cm or 2x2 cm), but we also went up to 4” wafers, all placed on a 6” Si carrier wafer without any thermal bonding. The carrier was oxidized with ~2 µm SiO_2 to limit reaction with the chamber plasma.

Our samples used 180 nm CSAR resist processed with e-beam lithography, except for the DOE test pieces which were 1.5 µm 5214e exposed with a maskless writer. All designs had a very low etch load (< 1%) and we have not paid attention to etch uniformity.

The Cr layer was deposited with Temescal at a rate of 1 Å/s and were between 15 and 40 nm thick.

DOE analysis

We did a design-of-experiment parameter sweep of the etching parameters with the range of values inspired by the default Cr etch recipe on the machine, recipes in literature, and recipes used by other users:

- Coil power: 300-500 W
- RF power: 15-25 W
- Total gas flow: 40-80 sccm (mixture of Cl_2 and O_2)
- Oxygen percentage: 15-25 %
- Pressure: 5-15 mTorr

The parameters were scanned according to a Plackett-Burman type distribution, including two center points. The result of the analysis is shown in Table 1. Figure 1 shows an example of the main effects on selectivity between CSAR resist and Cr.

Measurement details

For each parameter set, the “load & tune” was checked and coarsely improved when necessary. The etch rate was found by first stripping 20 nm Cr from a bare chip and monitoring through the window when the layer was gone, waiting an extra 5 seconds before stopping. The same etch also included a

Table 1 showing the effect of increasing the process parameter, e.g. higher pressure lead to higher selectivity while higher platen power (RF-power) lead to lower selectivity. Solid arrows had fit significance according to the analysis software, while the grey indicate small to no impact.

Outcome\parameter	*Pressure*	*Coil power*	*RF power*	*Flow rate*	*O2 %*
Selectivity	↑↑↑	↓	↓↓↓	↑	↑
Etch rate	↑↑	↑↑	---	---	↑
Sidewall angle	↑↑↑	↓	↓	---	↑
Bottom corner	↑↑↑	---	↓	↑	↑
Resist roughness	↑	↓	↑	↓↓	↑

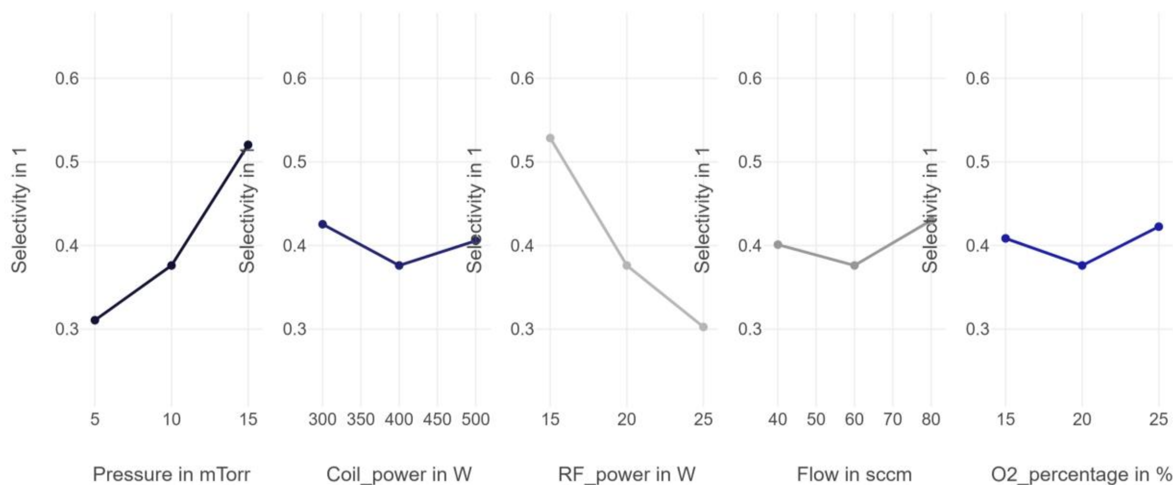

Figure 1 shows the main effects on etch selectivity between CSAR and Cr (CSAR:Cr). It is lower than one because the CSAR was always etched faster than Cr. Only pressure and RF power had a significant effect on the selectivity.

silicon chip with ~500 nm CSAR whose thickness was measured before and after to estimate the selectivity. We generally did not use crystalbond, but we tried it on some of our last tests where we found a ~10 % improvement in selectivity when adding the bond.

The other parameters were measured by etching gratings made with UV lithography and then investigating their cross-section with SEM. The “resist roughness” is a subjective rating from 1-5 of any deformation of the structure depicted in the SEM. The “bottom corner” is a rounding of the etched Cr profile near the sidewall, estimated from matching it to a circle and giving the radius in nanometer. The “sidewalls angle” was obtained with the built-in angle tool. Note that the resist sidewalls themselves has an angle which probably affects the Cr profile, and the chips were tilted by about 10 degrees from the perfect cross-section to show the depth, which also affects the accuracy of the measurement.

Observations

Pressure was by far the most impactful knob, and it looks like the etch should increase the pressure even beyond the considered range. Another interesting observation is the resist roughness; one parameter set clearly damaged the CSAR resist, making it look like frost on a windshield. That and the more roughened resist seems to correlate with high flowrate.
The DOE analysis suggest that the plasma interrogation time should be reduced from the starting STS recipe.

Testing the final Cr recipe

The final recipe that we settled on is:

mTorr	Coil (W)	RF (W)	sccm	O_2 %	Temp (C)	nm/min	Cr:CSAR
10	300	15	30	23	20	43	0.42

Ironically, this recipe uses a lower pressure than the default recipe which uses 15 mTorr. The reason was an unexpected problem depicted in figure 2:

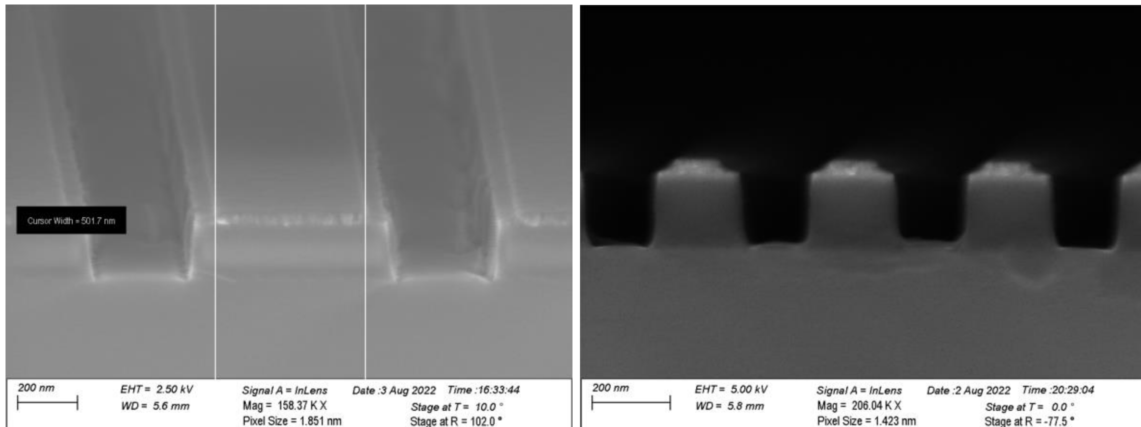

Figure 2 shows SEMs after Cr and nitride etching (using "a slow etch with carrier" on Metal ICP to remove nitride) for 20 mTorr during Cr etching.

Apparently, the Cr etches leaves some residues near the resist patterns, and that is enough to mask the nitride etch, making the sidewall incredibly uneven. An XPS analysis has both revealed CrO_2 and CrN left on the nitride surface after etching. That could cause the problem. Though it is unclear where these materials come from. It could be from the deposition chamber and material source itself, Cr binding to oxygen and nitrogen in the silicon nitride film, or as residue formed during or after Cr etching.

Solving the problem

We found two viable fixes to the problem in fig. 2 and have two more fixes that we have yet to test. First, one can increase the etch time to get a significant overetch, provided sufficient resist. Second, we have found that less overetch is needed when using a lower pressure, to the point where lowering the pressure is favorable although it leads to a larger Cr sidewall tilt. The third, untested, option is to add fluorine plasma etch to clear the surface before venting to atmosphere. We have found a Ph.D. thesis that claims this can help prevent CrN from being formed at the Cr etching. For the final, untested, step we have added a descum step prior to Cr etch because we found a considerable "tail" of resist after the e-beam lithography.

Final etch result

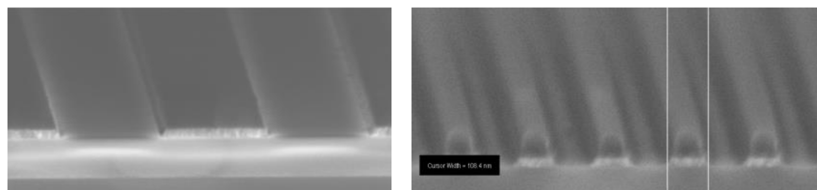

Figure 3 SEMs after Cr etch and (before) after resist strip on the (right) left. The CSAR sidewall on the right was very nearly vertical before Cr etch, indicating that the etch itself seems to add a tilt to the resist like the one in Cr.

Nitride etching with Cr hard mask

We chose to implement the new nitride etch recipe on the AOE because it is much less used than the Metal ICP. After some trial and error, included a failed DOE test (the tested parameter range was way to big) we settled on this recipe:

Coil (W)	Platen (W)	Temp (C)	He (sccm)	CF4 (sccm)	O2 (sccm)	Pressure (mTorr)	Etch rate (nm/min)
1300	350	5	174	40	4	4	420

This recipe is, essentially, the STS recommended recipe for etching nitride with resist mask, and then adding 4 sccm oxygen. The results are quite nice, e.g.:

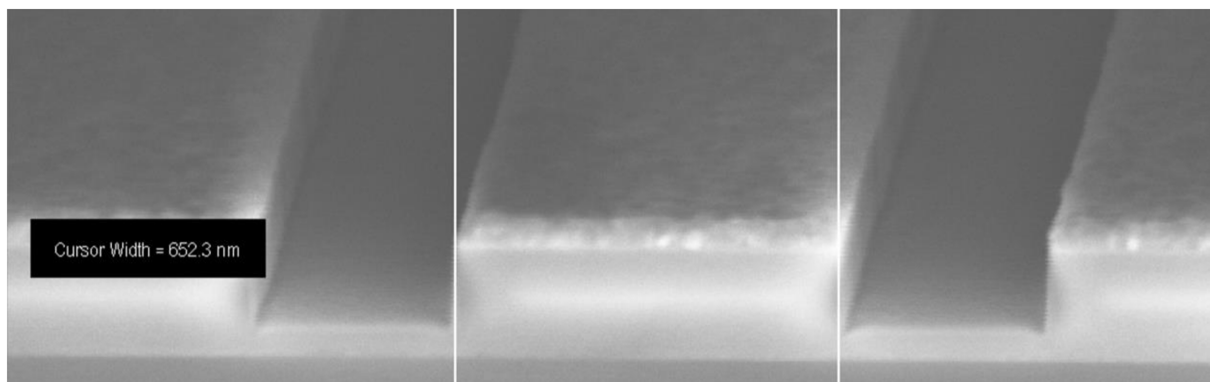

Figure 4 SEM of 200 nm thick, stoichiometric nitride plus 40 nm Cr hardmask on a silicon substrate after 20s etch with the new nitride recipe. The Cr thickness has grown with 5-10 nm due to formation of fluoride on the chromium.

One unforeseen complication is that the Cr mask is converted in CrFx during the etch, meaning the mask grows thicker before the Cr is removed, so it is not useful to talk about selectivity. Instead, we have measured the mask lifetime on 20 nm Cr chips to be 50s (although with significant edge-effects):

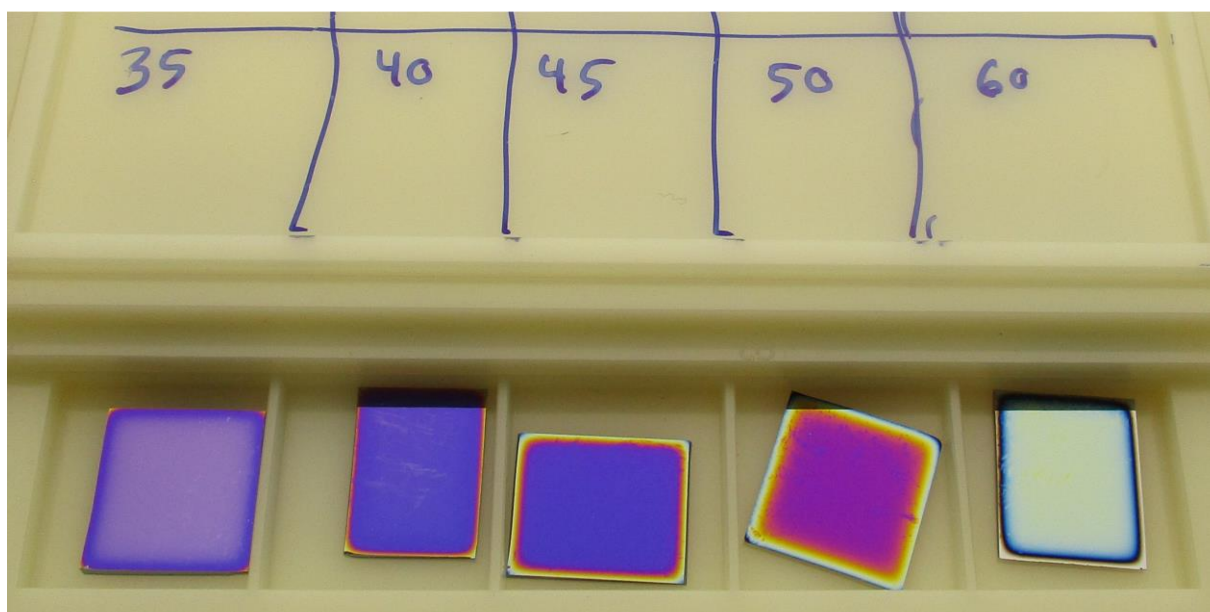

Figure 5 picture of chips with 200 nm nitride and 20 nm Cr after 35-60s of etching. The 50s still has all the nitride left.