Danmarks Tekniske Universitet

Micro-fabrication of x-ray optics

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Contents

1 Introduction

X-ray Talbot Interferometry (XTI) was first demonstrated by Momose in 2003, [Momose et al., 2003]. This X-ray imaging technique is fundamentally different from common techniques using phase-contrast measurement instead of attenuation measurement (absorption). This allows much higher resolution and detail level of X-rays images. One can easily realize the potential of this new technique in sectors where X-rays are already widely utilized. In the medical sector the technique can be used for higher contrast images of soft tissue where absorption images provides poor contrast due to the light elements found in the tissue, [Pfeiffer, 2012]. The phase-contrast imaging has also raised interest in the food industry where it can be used to detect small bones and other unwanted objects in processed food.

The technique requires spatially coherent X-rays, thus synchrotron radiation is the perfect choice for phase-contrast imaging, however, not a very practical choice for industrial applications. For incoherent light an optical grating G_0 can by inserted between the sample and the X-ray source. This setup was proposed by [Bech, 2009] and is illustrated on Fig. 1b, see next page. The XTI technique relies on the refraction of the X-rays interacting with matter exhibiting different refractive index, as opposed to the absorption technique which deals with the absorption coefficient of the matter. After traversing the sample, the refracted X-rays enters another grating, G_1, creating an intended phase-shift. This phase-shift creates a periodic interference pattern known as the Talbot effect. The Talbot pattern will repeat itself in certain distances, resulting in areas with high and low intensity. One wishes to measure the refracted X-rays in an area with high intensity but this results in poor contrast due to the non-refracted X-rays. These can be blocked off with a third grating, G_2, consisting of a periodic pattern of a highly X-ray absorbing material. A common choice of material is gold. Although gold is expensive, it is a well understood material when it comes to micro-fabrication processes.

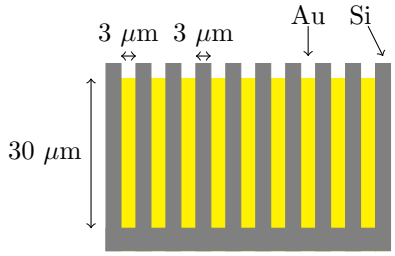
The goal of this paper is to test a fabrication process for the absorption grating, G_2, which is more simple than previous fabrication methods [David et al., 2007] and can be made in Denmark. The fabrication method in this project uses deep reactive ion etch (DRIE) and metal deposition followed by electroplating to fill the etched grating trenches with gold, see Fig. 1a on the next page. In order to verify the feasibility of the overall micro-fabrication process, a test grating is designed and produced. It consists of a chip on which a small grating is patterned and connected to a connector pad which will allow the electroplating of gold, see Fig. 2 on page 3.

2 Preparation

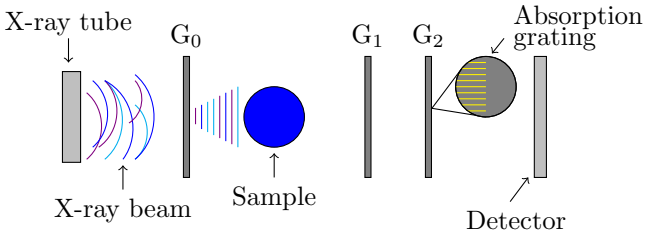
2.1 Design considerations

The grating can be seen in Fig. 1a and the setup in Fig. 1b.

Figure 1: The Figure shows a cross section of the absorption grating and its use in an experimental XTI setup.



(a) Cross section of the G_2 absorption grating micro-fabricated on a silicon wafer. The X-rays will enter the grating from the top.



(b) Experimental setup for XTI using 3 gratings serving different purposes including the absorption grating shown to the left, (a).

The line pitch of 6 μm ($2 \times 3\,\mu$m) is defined by the physical dimension of the final setup and the working Talbot distance. This dimension has not been investigated in this project and has been assumed constant. However, the height has to be evaluated. It is required that the absorption grating absorbs minimum 92% of the incoming X-rays in-between the periods of silicon where the gold layer is present. The intensity will be fully transmitted everywhere else, since silicon is almost transparent for the used X-rays. To evaluate the dimension to obtain this level of absorption, one can use equation (2.7) from [Bech, 2009] below.

$$I = I_0 \mathrm{e}^{-\mu r} \Leftrightarrow r = -\frac{\ln\left(I/I_0\right)}{\mu} \tag{1}$$

Where I_0 and I are the initial and transmitted intensities, usually measured in eV or counts pr. second, r is the travelled distance in the material and μ is the absorption coefficient in m^{-1}. The absorption coefficient is the inverse attenuation length found at [Benke et al., 1993]. The X-rays used in the setup have an energy of 25 keV, which corresponds to an attenuation length of 12.2427 μm for gold, thus the minimum required gold thickness can be evaluated as:

$$r = -\ln\left(0.08\right) / \left(12.2427\,\mu\mathrm{m}\right)^{-1} = 30.92\,\mu\mathrm{m} \tag{2}$$

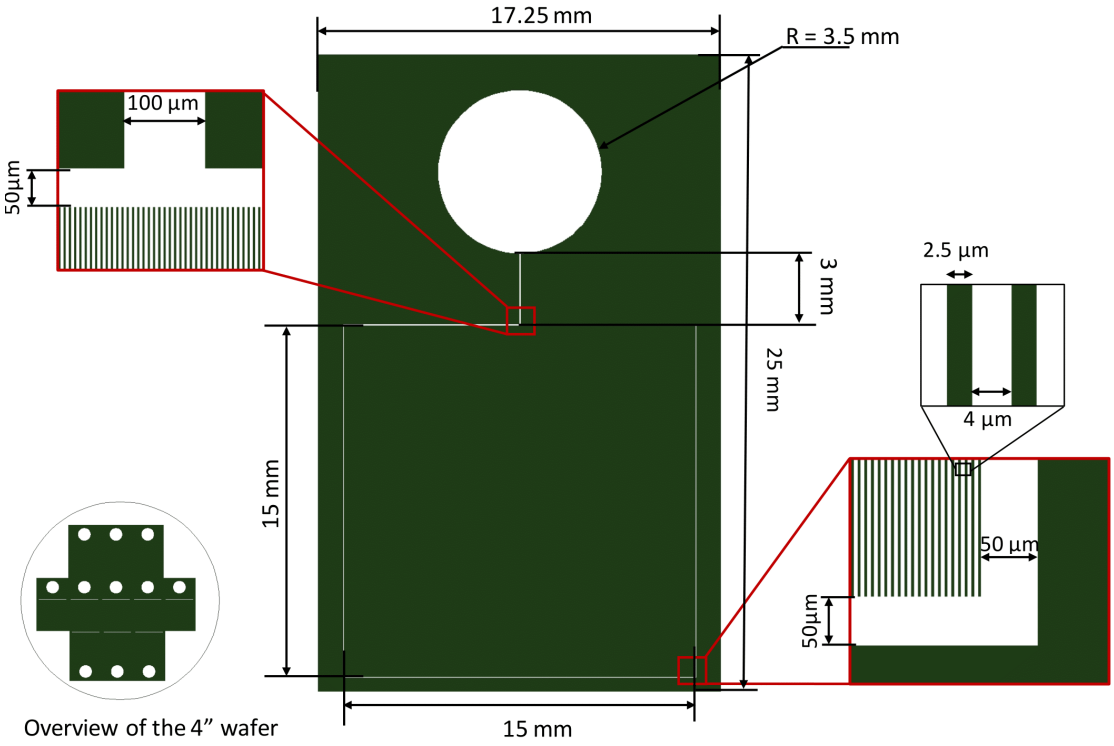
The spacing of the trenches in the G_2 grating is required to be 3 μm. This is to match the G_1 grating which produces the phase shift required for the setup. G_1 and G_2 pitch are related to each other by a geometrical factor defined by the setup dimension. The current fabrication process has shown that the technique used for the prototype fabrication of the G_2 grating produces incorrect sized spaces. A microscope image of a previous attempt to fabricate the G_2 grating can be seen on Fig. 17 in Appendix A.1. The etched trenches in this patterned silicon wafer were measured to be 2.24 μm wide and the silicons walls to be 3.64 μm thick, deviating substantially from the expected dimensions on Fig. 1a which is supposed to be $2 \times 3\,\mu$m. This large deviation is believed to be caused by the physical limits of the laser writer equipment (*Heidelberg maskless aligner*) when exposing the 1.5 μm thick photoresist. Some optimization could be performed, however they are time consuming and may not necessarily lead to the perfect ratio. Hence a correction in the design of +25.33 % for the gold etched channels must be made and likewise a

correction of -21.33 % for the silicon walls to obtain a 6 μm pitch with duty cycle of 1. These corrections are used in the designed photomask in the next section.

2.2 Photomask design

The mask design for a single chip is illustrated in Fig. 2. An overview of the mask design for the entire wafer can be found at the lower left corner. As can be seen, there are 11 chips on one wafer. Apart from the grating, each chip also has a border which is connected to a connector pad. This is 50 μm wide in order to conduct the electrical current along all the grating lines.

Figure 2: Photomask design. The green parts will be exposed to light. The photoresist is a reversed resist which means it will turn from a positive resist to a negative resist by a post-exposure bake, thus the green parts will remain and the white parts will be dissolved. Later the white area will be electroplated with gold. For further explanation see Fig. 4. Image credit: *Chantal Silvestre (DTU Nanotech)*.



2.3 Fabrication process

This section covers the fabrication process steps for manufacturing G_2. The detailed process flow is available in Appendix A.3. The absorption grating is manufactured on a 4" double side polished silicon wafer[1], this size allows up to 11 sample grating chips of 17.2 mm by 25 mm or one full sized grating of 6×6 cm. This wafer size is chosen because the used equipment at the DANCHIP cleanroom is optimized for this size.

[1]The wafer is in fact 100 mm, the term 4" is just a name.

2.3.1 Process steps

The fabrication of the grating will be done in 6 main steps. The list below contains a short description of the process. In Fig. 3 some of the steps corresponding to the enumerated list are illustrated. A more thorough review is found in the next sections describing what is going on in the most critical steps: Lithography and DRIE etching. For more practical details on the process see section 3 Cleanroom.

1. **Lithography**

   The grating design is transferred to the wafer.

2. **Dicing**

   The wafer is diced into small chips using a diamond pen.

3. **DRIE**

   The trenches are etched into the chips using the Bosch process.

4. **Metal deposition**

   Gold are deposited in the bottom of the trenches.

5. **Lift off and oxygen cleaning**

   The two polymers, the resist and the C_4F_8, are peeled off in an acetone bath and the chips are subsequently cleaned in an oxygen plasma to remove leftover polymer.

6. **Electroplating**

   The trenches are filled with gold by growing it from the deposited seed layer. This will be done by an external company.

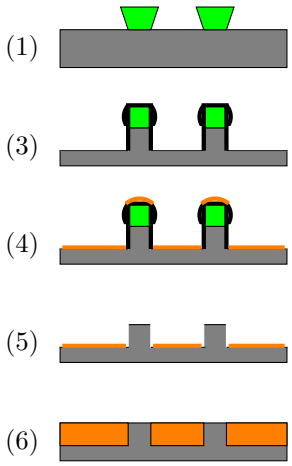


Figure 3: The figure shows the process steps described in the enumerated list. Orange (Au), Grey (Si), Black (C_4F_8) and Green (*Photoresist*).

2.3.2 Lithography

The first step of photolithography is coating the upside of the wafer in a photoresist chemical. First the wafer is baked to remove absorbed water which is followed by wafer priming where the wafer is coated in the chemical HMDS making the wafer slighty hydrofobic thus preventing reabsorption of water, [Franssilla, 2005]. The photoresist AZ5214E is chosen for the G_2 grating. This is a positive resist but with the attribute that it can be reversed as illustrated in Fig. 4. The *Gamma UV Spin Coater* coats the wafer by spinning it at a few thousand rpm (depending on the thickness) and applying a small amount of the photoresist at the center of the wafer so the photoresist is spread evenly across the wafer. The layer thickness is 1.5 μm which correspond to a spinning velocity of 5000 rpm for 30 seconds.

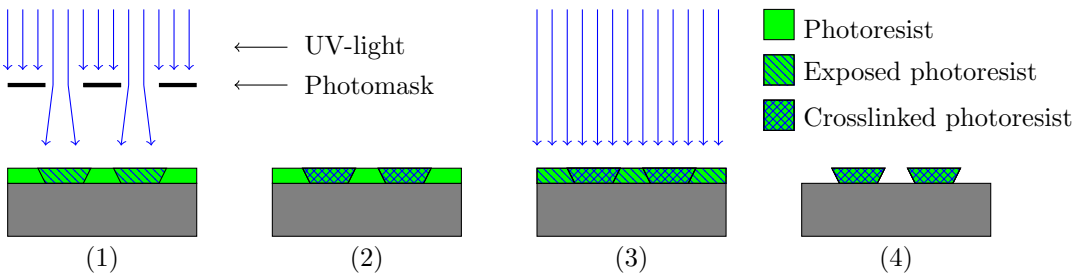


Figure 4: Illustration of a lithography reverse process, positive to negative.
(1) 1st exposure (2) cross-link bake (3) flood-exposure (4) developement

The photoresist can be exposed to UV light either through a photomask or by direct laser writing, also commonly known as a maskless aligner. The direct laser writing is chosen for the G_2 test chips, because this allows a higher degree of freedom for design change. If the design is found satisfying a physical photomask can be ordered, this is expensive and therefore only done when a final design is made. After the exposure of the photoresist one can choose to develop the resist directly, resulting in a positive pattern, or baking the photoresist and creating a negative resist, also called reverse process. Fig. 4 shows a negative photoresist reverse process.

1. The resist is exposed through a photomask or by direct laser writing. The polymer chains consist of carbon hydrates chains combined with photosensitive elements (DNQ - diazonaphthoquinone) resulting in long continuous chains of polymer. When exposed to light, the photosensitive element DNQ is destroyed leaving behind several broken polymer chains.

2. When baked the remaining polymer chains will receive enough energy to crosslink forming stronger bonds than the original polymer. In the crosslinked state, they will be resistant to light and the developer chemical because DNQ is destroyed.

3. The surface can now be flood exposed to UV-light. The polymer in the unexposed areas in (1) will now break while the cross-linked polymer will be less effected. This is the reverse step, [Franssilla, 2005]. The areas with broken polymer can now be dissolved in the developer.

4. The exposed area is developed in a TMAH (Tetramethylammonium hydroxide) based chemical developer. This is a highly toxic and corrosive chemical and should be handled with great care. This is used inside a sealed container for safety.

Before any further processing, the trenches dissolved in the resist should be inspected by optical microscopy. If the microscope images returns a trench dimension within $\pm 10\,\%$ of the expected 3 μm they can be further processed and diced.

2.3.3 Etching

In the next step of the fabrication process, the grating pattern is transferred to the silicon by etching the areas without resist. There are two types of etching: dry etching and wet etching. Wet etching uses wet chemicals to make the silicon soluble and as such removable. This process is usually highly isotropic, meaning that it will etch in all directions. Dry etching is also isotropic but can be made anisotropic with special processes. Anisotropic means that the etching is higher in a specific direction. The etchant in dry etching is often a plasma of for example ions which can bind to the silicon and make volatile by products, [Franssilla, 2005].

An anisotropic etchant is preferred for etching the gratings seen in Fig. 1a. An example of a plasma etching is RIE (*Reactive Ion Etch*) where reactive ions are bombarded to the silicon surface. We will be using a special RIE technique called DRIE (*Deep Reactive Ion Etch*). DRIE is useful for etching narrow and deep trenches and thus suitable for the fabrication of the grating. The advantages of DRIE over RIE is the high etch rate and the ability to create deeper trenches. To achieve an anisotropic etching one can use the Bosch process, a DRIE etch process which consists of a two-step cycle. First the silicon is etched, next a protective fluoropolymer (C_4F_8) is deposited. This cycle is repeated until the desired dept is reached. The Bosch process is illustrated in Fig. 5 on the next page.

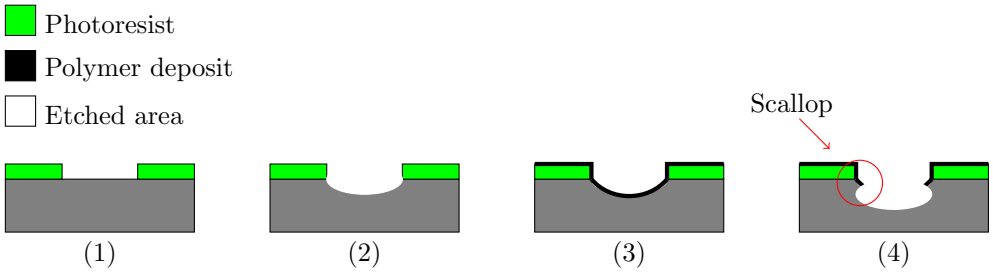


Figure 5: The Bosch process

1. Parts of the photoresist has been dissolved by the developer and leaves the silicon bare (1).
2. The fluorine ions in the SF_6 plasma can attack the bare silicon etching a few microns creating an isotropic etch seen on (2).
3. The flow of SF_6 plasma is cut and the wafer is covered in a protective fluoropolymer C_4F_8 (3), [Franssilla, 2005].
4. A new cycle of plasma etching. A potential difference over the wafer will cause the ions to be drawn towards the bottom and therefore the etching will be focused downwards, making a new isotropic etch.

Multiple cycles will create an anisotropic etch with residues of the protective polymer on the sidewalls of the trenches. Each cycle will create scallops on the sidewalls due to the isotropic etch before the protective polymer deposition. An illustration of a scallop is marked in Fig. 5.

In wet etching it is not possible to direct the etch by applying a potential difference.It would also be more difficult to control the etching.
Due to the cyclic nature of the DRIE process, small bumps of C_4F_8 polymer will accumulate at the top of the pit because the polymer is continuously dumped here as the number of cycles increases. One might think of these bumps as a problem because they make the walls less vertical but it turns out that they are an advantage for the deposition of the metal seed layer at the bottom of the trench, because they shade the walls so that no gold will be deposited here. This is an advantage because the trench will be as clean as possible for the electroplating. Since the bumps are made of polymer they can be removed with acetone and oxygen plasma without harming neither the seed metal layer nor the silicon.

3 Cleanroom

In this section we will go through the equipment and practical procedure for the fabrication of the G_2 test chip. The whole fabrication process was carried out inside the DANCHIP cleanroom. It is an ISO 9001-certified cleanroom located at the DTU campus [Danchip, 2017].

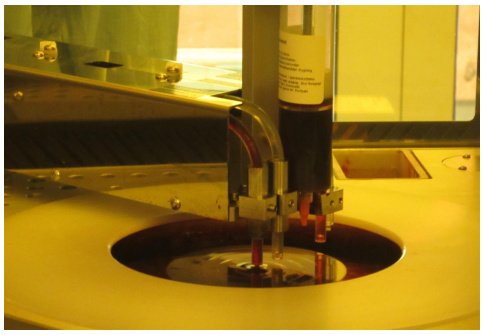
3.1 Lithography

The wafer used for fabricating the grating was a n-type 4" wafer (Box Nr.*ON528*), DSP[2] 350 ± 15 μm. The photolithography process starts out by applying the photoresist. The chosen photoresist program is the *AZ5214E 1.5um with HMDS* run by the *Gama UV Spin Coater*. The whole process of prebaking, HMDS-doping and spincoating was carried out automatically inside

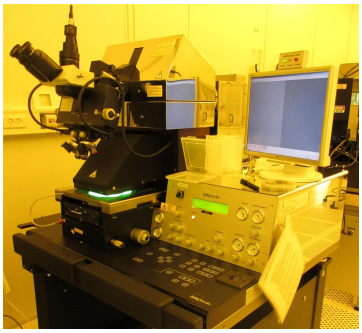
[2]Double side polish

the machine. A picture of the spin coating in process can be seen in Fig. 6a. The pattern was transferred onto the photoresist by the *Maskless aligner 01 (Heidelberg)*. After transferring the pattern a reversal bake was carried out on a hotplate by running the program sequence *DCH PEB 110C 120S* baking the wafer for 120 seconds at 110 °C.This causes the previously exposed area to cross-link.

Figure 6: Pictures from the fabrication.



(a) Spin coating in progress



(b) Aligner machine performing flood-exposure.

The flood-exposure was performed by the *KS Aligner* without a mask for 30 seconds. The power of the light was set to 7 mW/cm^2. A similar machine can be seen in Fig. 6b. The last part of the photolithography is developing the resist. The *Developer: TMAH UV-lithography* was used for this purpose. The selected sequence was *DCH 100mm SP 60*. Meaning the wafer was developed in TMAH in a single puddle for 60 seconds. Before developing the pattern was not visible on the wafer yet. In Fig. 7 there is a before and after picture of a pattern being developed. This grating design is an earlier design and not the one used for the results. Grating Design credit: Chantal Silvestre.

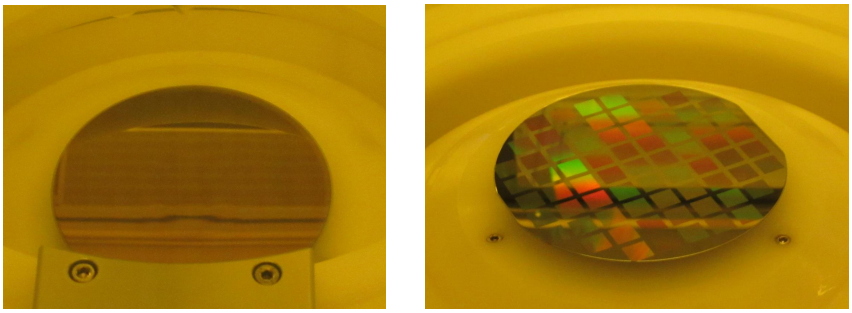


Figure 7: TMAH Developer before (left) and after (right).

3.2 Dicing

The individual chips on the wafer were isolated by dicing the wafer inside a dedicated fume hood. First a diamond pen was used to draw a line on the wafer. Next the wafer was snapped along this line. This is possible because the silicon atoms are bound in a crystal lattice. The approach is illustrated on Fig. 8 on the next page.

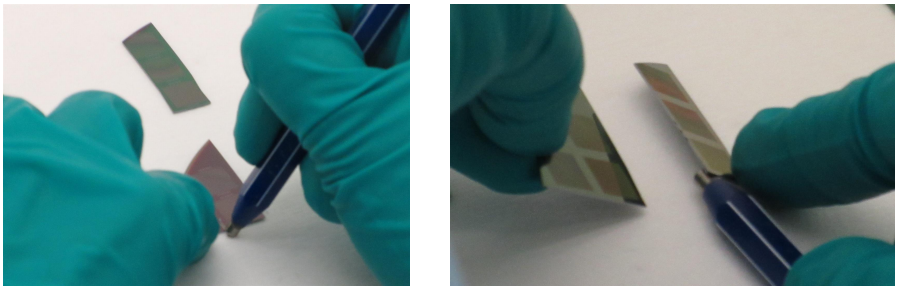


Figure 8: Dicing procedure. Left: Use a diamond pen to scracth a line. Right: Snap along this line.

3.3 DRIE

The etching of the silicon was done inside the *DRIE-Pegasus* at -19°C using the Bosch process described in Section 2.3.3 Etching. In order to load the chips into the machine, they had to be attached to a 4" wafer. This was done using a vacuum oil. In Fig. 9 some test gratings are placed on a wafer using this oil. The program run on the Pegasus was the *DREAM_3um* recipe with 100 cycles.

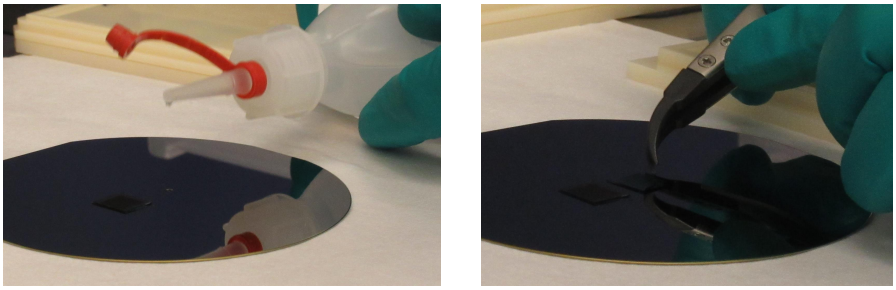


Figure 9: Placing the chips on a 4" wafer using a vacuum oil.

The etch time was 9 min and 37 seconds which created a trench with a depth of 32um, thus an etch rate of 3.3um/min. See Fig. 12a for this result.

3.4 Metal deposition

The metal deposition was done inside the *Metal evaporator - Wordentec* machine. The base pressure was 2.1×10^{-6} mPa, which is a very high vacuum although a lower pressure was desired for more directional diffusion. 10 nm of titanium and 70 nm gold were deposited. A before and after picture can be seen in Fig. 14a

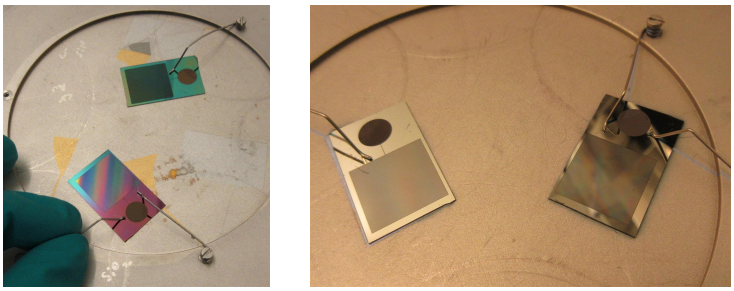
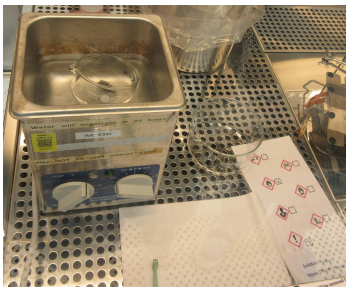


Figure 10: The G_2 grating chips before (left) and after (right) gold deposition

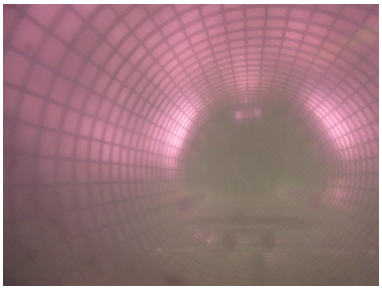
3.5 Lift-off and plasma clean

The final step was to remove the polymer. This was done using an acetone bath and an oxygen plasma. In the acetone bath, most of the polymer was peeled of, but to remove the last remains it was necessary to plasma ash the chips using the *Plasma Asher 1*. In Fig. 11a there is a picture of the acetone bath setup and in Fig. 15 the plasma ashing chamber.

Figure 11: Removing polymer.



(a) Set-up for the lift-off: The chips are placed in a heated acetone water bath and afterwards cleansed in isopropanol.

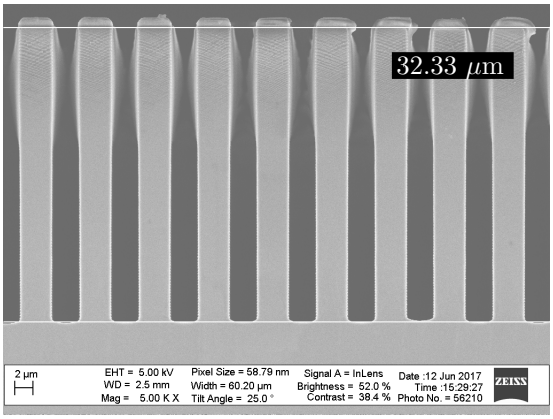


(b) The plasma ashing chamber. The plasma consists mainly of O_2 and a bit of N_2. The chips were placed on a 4" wafer but not glued to it because the wafer doesn't move.

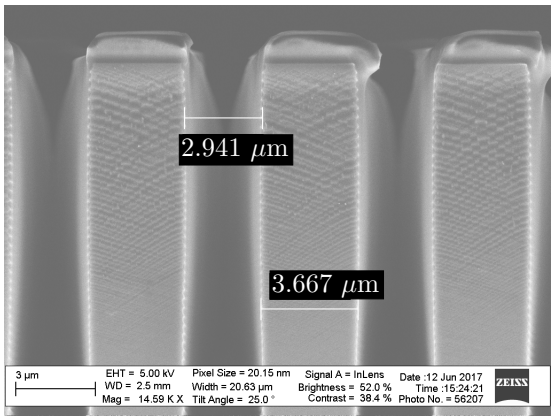
4 Results

The final G_2 test chip was fabricated as described but an additional chip with 30 seconds development time was also made. This had a better pitch than the 60 seconds chip, pictures of this chip can be found in Appendix A.2 Fig. 18. Thus the 30 seconds chip will be the main result. The following pictures of the final grating chip were produced by Scanning Electron Microscopy (SEM) for higher resolutions compared to optical microscopy. The microscope used was the *SEM Supra 1*. In Fig. 12 one can see an overview of the cross-section of the trenches and a close-up used for distance measurements.

Figure 12: A cross-section view of the trenches before metal deposition.



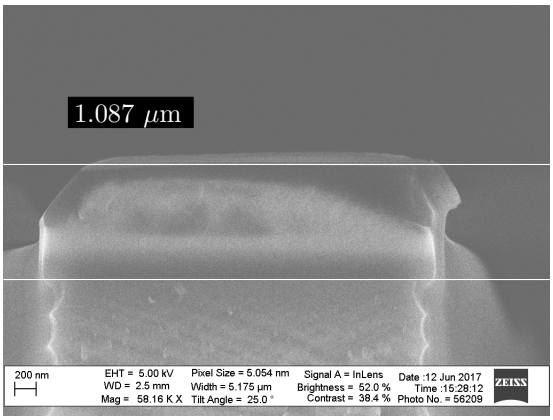
(a) The dept of the trenches were measured to 32.33 μm, thus enough gold can be deposited for the desired shielding.



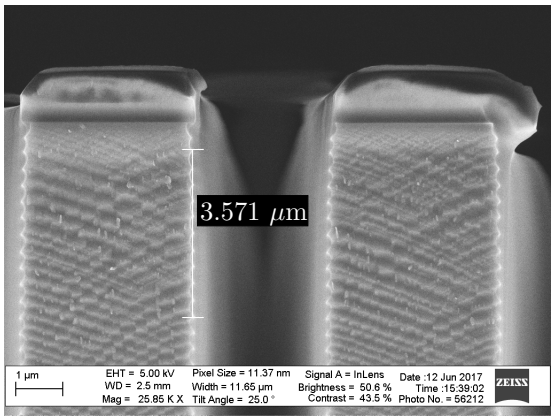
(b) The width of the sidewalls are a bit off due to the build-up layer of protective fluoropolymer.

In Fig. 12b the pitch is measured to be $2.9 + 3.7$ μm instead of 6 μm which is too big but upon closer inspection of the picture one can see the wrong size is due to the build-up layer of protective fluoropolymer. The build-up is thicker closer to the surface of the trench due to the many cycles in the Bosch process. Fig. 15 shows the chip after lift-of and the pitch for this picture is commented on after the picture.
In Fig. 13b the scallop size is calculated by measuring the length of 10 scallops and calculating an average. Thus one scallop and therefore one iteration of the Bosch process is approximately 0.36 μm in agreement with Fig. 12a showing 100 cycles created a 32.33 μm deep trench.

Figure 13: A closer inspection of the photoresist and scallop size.



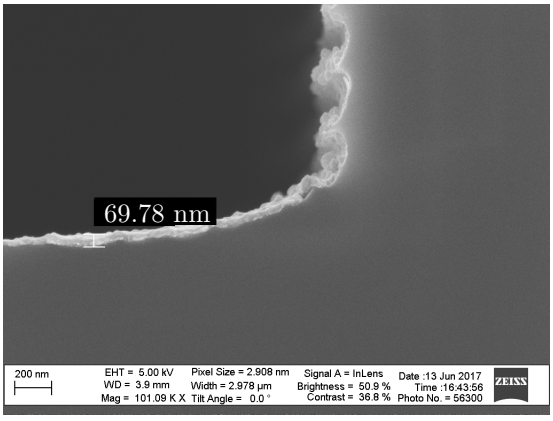
(a) Measurement of the photo resist layer.



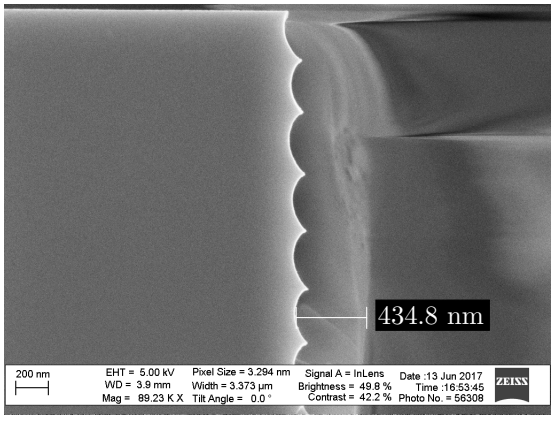
(b) Measurement of the scallop size.

The thickness of the photoresist was measured to 1.09 μm in Fig. 13a, thus slightly thinner than the expected 1.5 μm. This is due to the DRIE etch which has etched some of the photo resist as well. This is of no concern since the resist will be removed in the lift-off anyways.

Figure 14: An inspection of the deposited gold layer and polymer build-up.



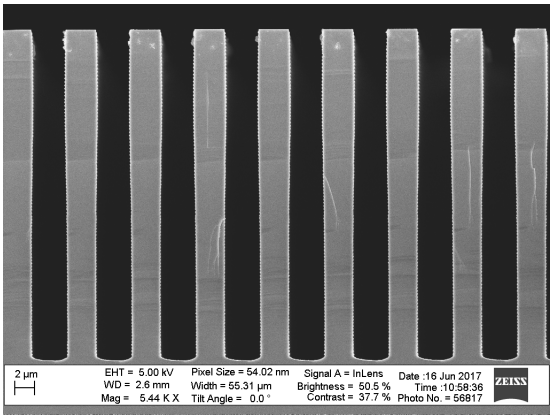
(a) A close inspection of the seed gold layer.



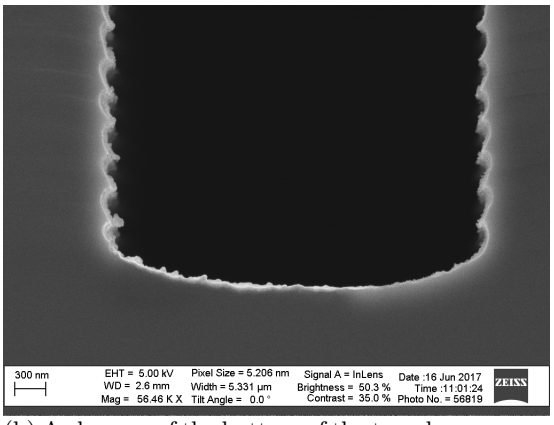
(b) A close inspection of the build-up fluoropolymer layer. Notice that there are no gold on the sides, meaning the bumbs shadowed the walls perfectly as hoped.

In Fig. 14a the deposited gold layer is measured to a thickness of 69.78 nm. This is very close to the 70 nm meant to be deposited. Therefore this part of the fabrication process is regarded as successful. In Fig. 14b the build-up layer of fluoropolymer was measured to a thickness of 434.8 nm, this is too thick and must be removed otherwise the trenches it may interfer with the electroplating. This also explains the large size measured in Fig. 12b. In Fig. 15 the polymers have been lifted off and cleaned with plasma ashing. By a quick inspection one can see the trenches appear much straighter in 15a compared to 12a.

Figure 15: The final result after lift-off and plasma ashing.



(a) A crossview of the ashed trenches.



(b) A close up of the bottom of the trench. The bright area in the bottom is the gold.

During the SEM the trench width was not measured with the SEM-software , but the pictures included a scale to pixel ratio. In the program ImageJ this scale was used to measure the width of the trench in Fig. 15a to 3.16 μm and the sidewalls to 3.29 μm. This is within the acceptable boundary of ± 10 % to the expected 3 μm and certainly much better than the prototype in Appendix A.1 in Fig. 18. Therefore one can conclude that the pitch adjustment was successful but can still be improved.
In Fig. 15b an asymmetry reveals itself at the bottom of the trench: There is more gold deposited on one side of the trench than the other. We suppose that this asymmetry is related to scattering during the gold deposition. A lower pressure in the deposition chamber might improve this, but to test this requires further investigation. Also, it was not possible to electroplate the test wafer during the scope of this project as it is performed by an external partner, so whether this will work is also up to further investigations.

5 Perspective discussion

The proposed fabrication has proved to be feasible for the performed steps. The pitch length and trench depth were within an acceptable boundary of ± 10 % for this project. Furthermore the complexity of the fabrication has been greatly reduced compared to [David et al., 2007]. In this paper the fluoropolymer bumps was used as advantage during the deposition of the gold seed layer. In [David et al., 2007] wet etch was used and bumps were created using a deposition of aluminum, which is significantly harder to do than using the Bosch process. The Bosch process also has the advantage of speed which is a key factor in industrial applications. The electroplating of the gold was not done, therefore this can not be compared to other fabrication processes. One might propose the use of tungsten instead of gold since they have similar X-ray absorbing properties but have a vastly different price. A quick calculation reveals that the cost of the gold for a 6 cm $\times$ 6 cm grating is 45.2 $ compared to only 0.3 $ for tungsten, see the code

in Appendix B.1. Using absorption data from [Benke et al., 1993] one can compare the required shielding thickness using equation (1), note here that the absorption coefficient is dependent on energy. A plot of the shielding thickness as a function of photon energy can be seen below in Fig. 16.

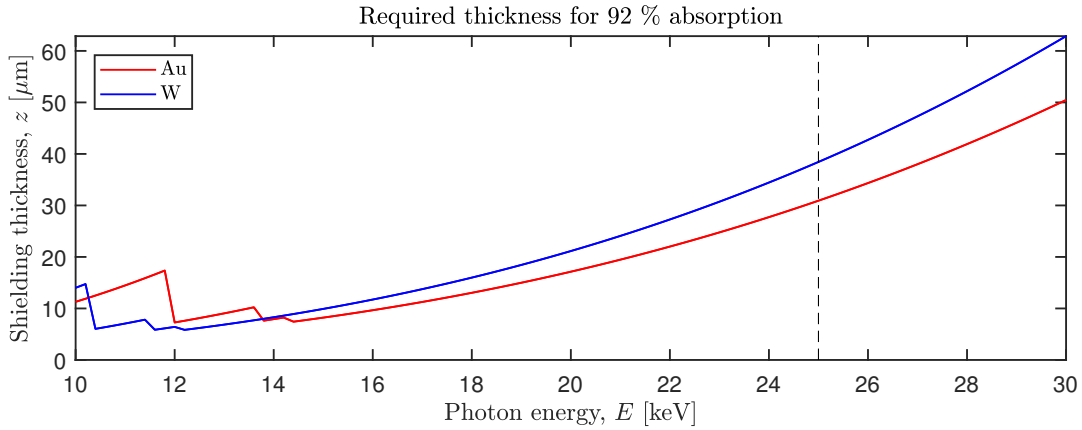


Figure 16: The required shielding thickness for gold and tungsten for different photon energies. The irregularities around 10-12 keV is the absorption edges.

The code for the plot can be found in Appendix B.1. The plot reveals that 30 μm trenches are too shallow for higher energies around 30 keV, thus the grating cannot be used for shorter X-rays. One might also consider a total different fabrication process where a tungsten wafer is used instead of a silicon wafer. Here one only needs to etch non-absorbing trenches into the tungsten wafer thus greatly simplifies the fabrication and reduces cost. In the final setup monochromatic X-rays are not used and one needs to consider that the energy of the X-rays might be in the range of 25 ± 2.5 keV, as seen in Fig. 16 this requires a slightly thicker shielding of 40 μm for gold and 50 μm for tungsten. Therefore the dept of the trenches in fabricated grating might not be deep enough too shield the X-rays.

6 Conclusion

The fabrication process for the absorption grating G_2 was tested and found successful. The process allowed a simpler fabrication of the grating compared to [David et al., 2007]. The DRIE etch proved to be a feasible process ensuring gold deposition to only be at the bottom of the trench. The trenches were straight and correct sized within ± 10 % of the desired pitch, see Fig. 15a. This leaves room for further improvement, but one can still conclude that the correction made in Section 2.1 was successful compared to Fig. 17 found in Appendix A.1. The fabrication process was only tested for small chips and therefore the final grating with a size of $6\,\text{cm} \times 6\,\text{cm}$ needs to be tested. The final step of electroplating was not done in time and thus no conclusion about this part can be made. Further investigation can also be made in substituting gold with tungsten for price reduction. Therefore one can conclude that the goal of this paper has been reached but with room for further improvement and future investigations.

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Atsushi Momose, Shinya Kawamoto, Ichiro Koyama, Yoshitaka Hamaishi, Kengo Takai, and Yoshio Suzuki. Demonstration of x-ray talbot interferometry. *Jpn. J. Appl. Phys.*, 42(7B): L866–L868, 2003.

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A Appendix

A.1 Prototype fabrication

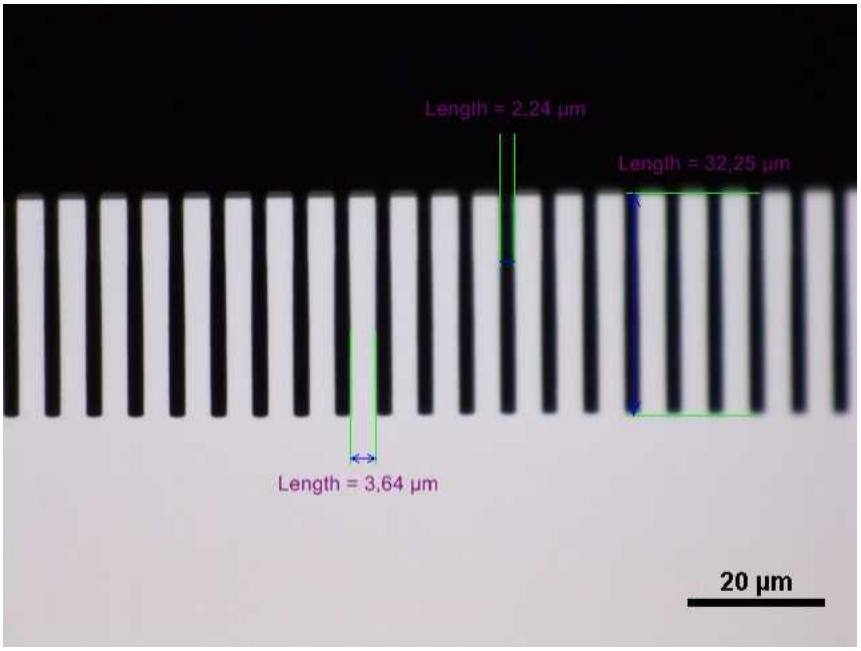
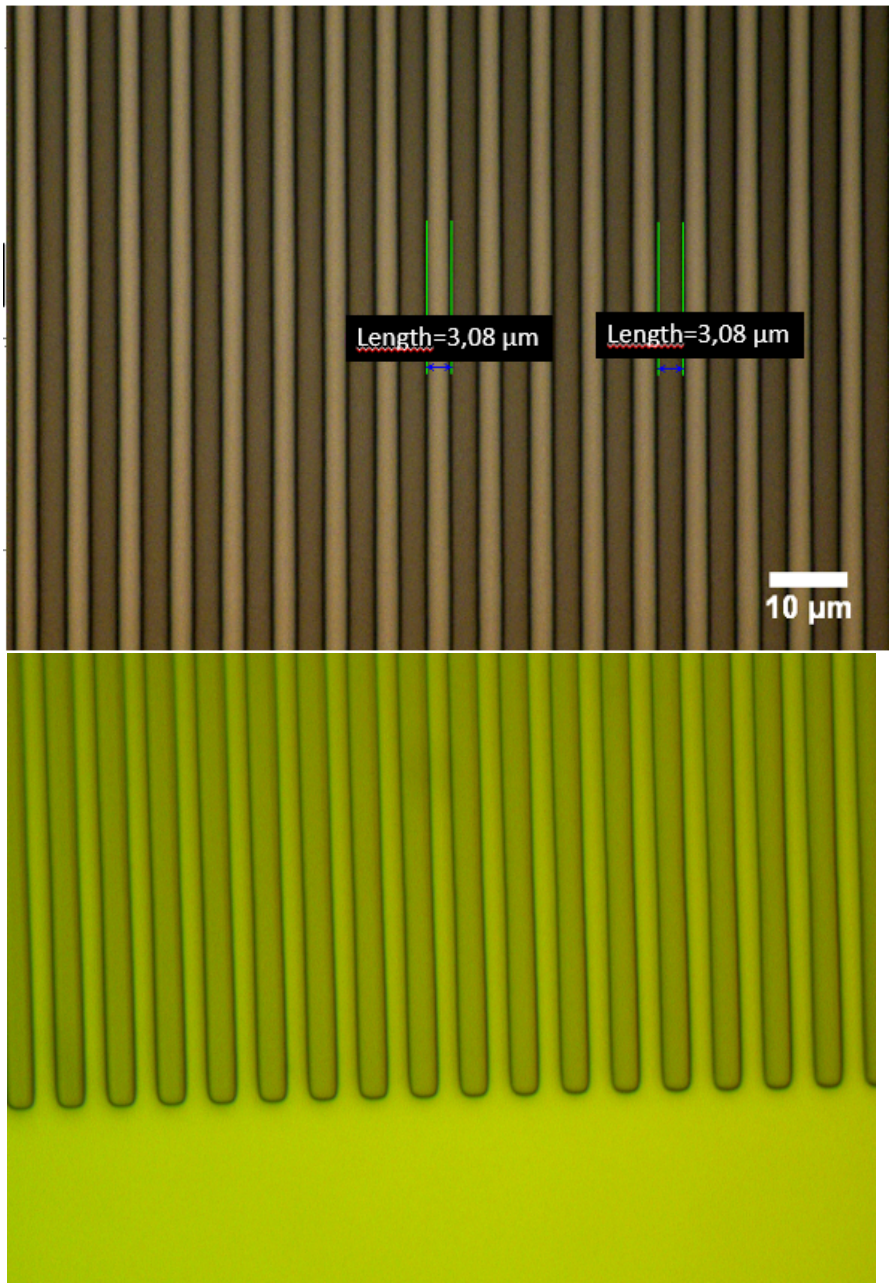


Figure 17: Prototype technique attempt performed prior this project. Microscope image,just after the DRIE step, of a $3\mu m$ grating with what was supposed to be a duty cycle of 1:1. The C4F8 layer is not visible with this resolution.The wrong duty cycle is believe to be due to the lithography step performed with the maskless aligner.

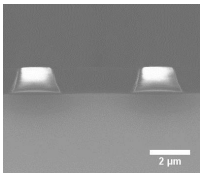
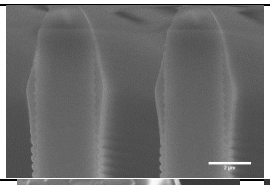
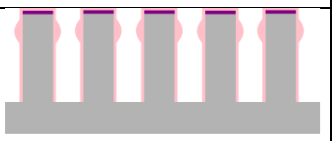
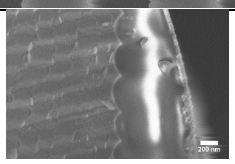
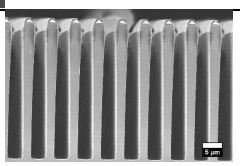
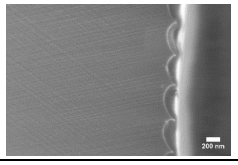
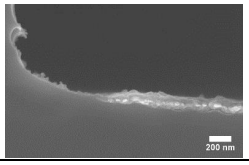
A.2 Development time

Figure 18: Comparison of development time. Top: 30 seconds development time in TMAH. Bottom:60 seconds development time in TMAH. Scale same as top one.

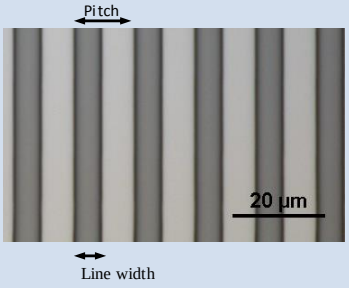


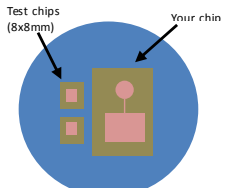
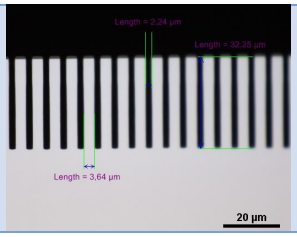
A.3 Process flow

Process flow title			Revision
Electroplating of trenches with seed layer			**1.0**
DTU Danchip National Center for Micro- and Nanofabrication	Contact email chasil@danchip.dtu.dk	Contact person Chantal Silvestre	Contact phone 52769482
	Group Silicon Technology / Batch name	Date of creation 25-04-17	Date of revision 01-06-17

Caption	Expected result *(from previous experiment).*	Figure
Resist patterning AZ5214e, 1.5um		
DRIE		
Metal deposition (thermal evaporation)	   	
Polymer removal		
Electroplating		

Process flow title	Rev.	Date of revision	Contact email
Electroplating of trenches with seed layer	**1.1**	01-06-2017	chasil@dtu.dk

Step	Heading	Equipment	Procedure	Comments
1	**Wafer selection**			
1.1	Wafer	Shelf	ON528 or ON516 n-type/Phosphor Resisitivy 1-20 Ωcm <100> DSP 350 ± 15 µm Price 283 DKK/pce	Remember to buy them in LM if you take the wafer from the shelf. NOTE : wafer box number may change
2	**Resist spinning**			
2.1	Spin resist	Gamma UV spin coater	AZ5214E 1.5um with HMDS	
2.2	Mask exposure	Maskless aligner	**Focus** : -4 **Dose** : 200 mW/cm^2 **Mask** : your own mask design	File format must be .gdsII The total exposure is controlled by the machine. You do not need to worry about the time.
NOTE: it is important that the wafer is not exposed to the white light of the cleanroom. Stay in the yellow area after you have exposed until you have developed (step 4). If you are using the equipment mentioned bellow, you should not have to cross any white are of the cleanroom, but if for some reason that should be the case, please use a black transport box.				
2.3	Reversal bake	Developer: TMAH UV-lithography	**Reversal bake:** 120 s @ 110 °C **Sequence:** DCH PEB 110C 120s	This is just a "bake" on the hot plate to induce cross-link of the polymer. PEB stands for Post Exposure Bake DCH stand for DanCHip
2.4	Flood Exposure	KS Aligner	**Mask** : none **Exposure mode** : Flood-exposure **Exposure time** : 30 s @ 7 mW/cm^2 (Exposure dose : 210 mJ/cm^2)	The energy of the light is fixed to 7 mW/cm^2 Thus, an exposure of 30 seconds will give a dose of 210 mJ/cm2.
2.5	Develop	Developer: TMAH UV-lithography	**Development in TMAH**: single puddle, 60 s **Sequence:** DCH 100mm SP 60s	This is the development of the resist which has been exposed. After this step, the pattern is visible on the wafer.
3	**Characterization**			
3.1	Line width measurement	Microscope NIKON	Magnification 100x	Measure the line width and the line pitch with the magnification 100x. Remember to press on "Y" to print the scale and dimension on the image before saving the image. Move to magnification 100x step by step. On the image : light gray is Si and dark gray is resist  Feel free to take image of other things you may find interesting! (ex. Structures that look weird, overall image of the pattern,...)
4	**Dicing**			
4.1	Dicing	Fumehood : special purpose	Cleave the wafer with a diamond pen. Store each of the chip in a single 2" carrier wafer.	

5	**DRIE**			
5.1	Change temp. chuck	Pegasus	**Recipe :** change temp / temp -19C	We have a better control of the etch rate when temperature is low. Therefore, we run the dry etch at a chuck temperature of -19C Change temperature chuck to -19C
5.2	Cleaning/conditioning	Pegasus	Load dummy Si wafer in the machine **Recipe** : Clean_DREAM **Time** : 15 min	Clean_DREAM is an oxygen clean use to create a conditioning of the machine. It has been observed on previous tests that running this recipe just before the main etch, allows for a better reproducibility of the dry etch pattern from one time to another.
5.3	Cleaning/conditioning	Pegasus	Unload the dummy wafer from the chamber	
5.4	DRIE	Pegasus	**Recipe** : DREAM_3um **Number of cycle** : 100 cycles	Bond two 8x8mm, 3um chip next to your sample on an alumina (Al_2O_3) wafer. Use a tiny drop of Fomblin oil to bond the chip. The 8x8mm, 3um sample are available on my shelf in single carrier chip box. We will use this chip to measure the depth of the etch. Drawing is not to scale, but it will more or less look like that once you have bonded the chip to the alumina substrate. 
5.5	Clean	Pegasus	Unload the wafer Run cleaning chamber Recipe : TDESC 20min	You can remove the chip from the surface of the wafer by just sliding them out of the wafer with a twizer.
6	**Characterization**			
6.1	Depth etch	Microscope NIKON	Cleave one of the test chip 8x8mm in the orientation perpendicular to the grating. Mount the cleaved chip on a 90deg holder to look at the trench in the microscope. Magnification 100x	
7	**Metalization**			
7.1	Metalization	Wordentec	Ti : 10nm Au : 70nm	Mount the second test chip and the sample onto a holder for small sample.
8	**Lift-off**			

8.1	Lift-off	Acetone bac	Fumehood : lift-off	Acetone bath until lift-off done (~7 min) Isopropanol bath for ~30 sec Rinse in DI water.
8.2	Oxygen clean	Plasma asher	Run recipe 18 Time : 30 min	After lift-off, some of the C4F8 remain unpeeled. The oxygen plasma will etch it, thus making the chip cleaner.
9	Characterization			
9.1	Characterization	SEM I	Cleave test wafer and look at the trench in the SEM. We should be able to see a Au seed layer at the bottom of the trench.	

B Appendix

B.1 Matlab code

```
%% Shielding
% Loads mass attenuation coefficients  (Source:CXRO)
Au = load('Au.txt');   % [eV, attenuation length microns]
W = load('W.txt');

% Calculates absorption coefficient
Au(:,2) = 1./Au(:,2);
W(:,2) = 1./W(:,2);

% Calculates thickness in microns
zAu = -(log(0.08)./Au(:,2));
zW = -(log(0.08)./W(:,2));

% Converts units to keV
Au(:,1) = Au(:,1);
W(:,1) = W(:,1);

% Plots results
figure(1)
set(1,'DefaultTextInterpreter', 'latex')
plot(Au(:,1)./1000,zAu,'r-','Linewidth',1)
hold on
plot(W(:,1)./1000,zW,'b-','Linewidth',1)
hold on
plot([25 25],[0 max(zW)*1.2],'k-')
title('Required thickness for 92 \% absorption','Interpreter','latex')
xlim([10 30])
ylim([0 max(zW)])
xlabel('Photon energy, $E$ [keV]')
ylabel('Shielding thickness, $z$ [$\mu$m]')
lgd = legend('Au','W','Location','northwest');
set(lgd,'Interpreter','latex')
set(gca,'fontsize',12,'linewidth',1.0)

% One calculation
% Multiplication by attenuation length in microns
thicknessAu = -log(0.08)*12.2427
thicknessW = -log(0.08)*15.2208

%% Price calculations
% Calculate the volume, Vol = height*width*length*numberOfTrenches

VAu = (thicknessAu/10000)*3e-4*6*(6/(6e-4));
VW = (thicknessW/10000)*3e-4*6*(6/(6e-4));

% Density
rhoAu = 19.32;   % [g/cm^3]
rhoW = 19.3;     % [g/cm^3]

% Mass
MAu = VAu*rhoAu;  % [g]
MW = VW*rhoW;  % [g]

% Price: 42000$ per kilo Au and 200$ per kilo W
priceAu = MAu*42000/1000
priceW = MW*200/1000
```