STS DRIE Etch Results for Danchip MP0636 Field Acceptance

21st April 2010

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Abstract

The following processes form the basis of customer field acceptance for the Pegasus^{ASE} etcher MP0636. Process A and B were run on 150mm STS wafers while process C and D were run on customer supplied wafers

- Process A – Large trench (80µm) 150µm depth.
- Process B – Via (30µm) 100µm depth.
- Process C – Nano silicon etch.
- Process D – Micro stamp silicon etch.

The process conditions and results are outlined in this document.

Acceptance processes

The aim of this document is to provide process conditions and results achieved during field acceptance at Danchip (DTU, Denmark) of MP0636.

Process A: (80µm Trench)

- ER (µm/min): > 15
- Depth (µm): 150
- Scallops (nm): <800
- Profile: 91 +/- 1
- Selectivity: > 150
- Undercut (µm): <1.5
- Uniformity (%) <3.5
- Repeatability (%): <4

Process B: (30µm Via)

- ER (µm/min): > 10
- Depth (µm): 100
- Scallops (nm): <800
- Profile: 91 +/- 1
- Selectivity: > 100
- Undercut (µm): <1.5
- Uniformity (%) <3.5
- Repeatability (%): <4

Processes to be demonstrated on 150mm STS type-S wafers.

Acceptance processes continued

Process C: "Nano etch"

- ER (nm/min): NS
- Depth (nm): 300
- Scallops (nm): <30
- Profile: 85 +/- 5
- Selectivity: NS
- Undercut (nm): <30
- Uniformity (%) <3.5
- Repeatability (%): <4

Process D: "Micro stamp etch"

- ER (µm/min): NS
- Depth (µm): 20-30
- Scallops (nm): <30
- Profile: 85 +/- 5
- Selectivity: NS
- Undercut (nm): NS
- Uniformity (%) <3.5
- Repeatability (%): <4

Processes to be demonstrated on 100mm wafers provided by Danchip.

Process A

80µm Trench

(STS 150mm wafers)

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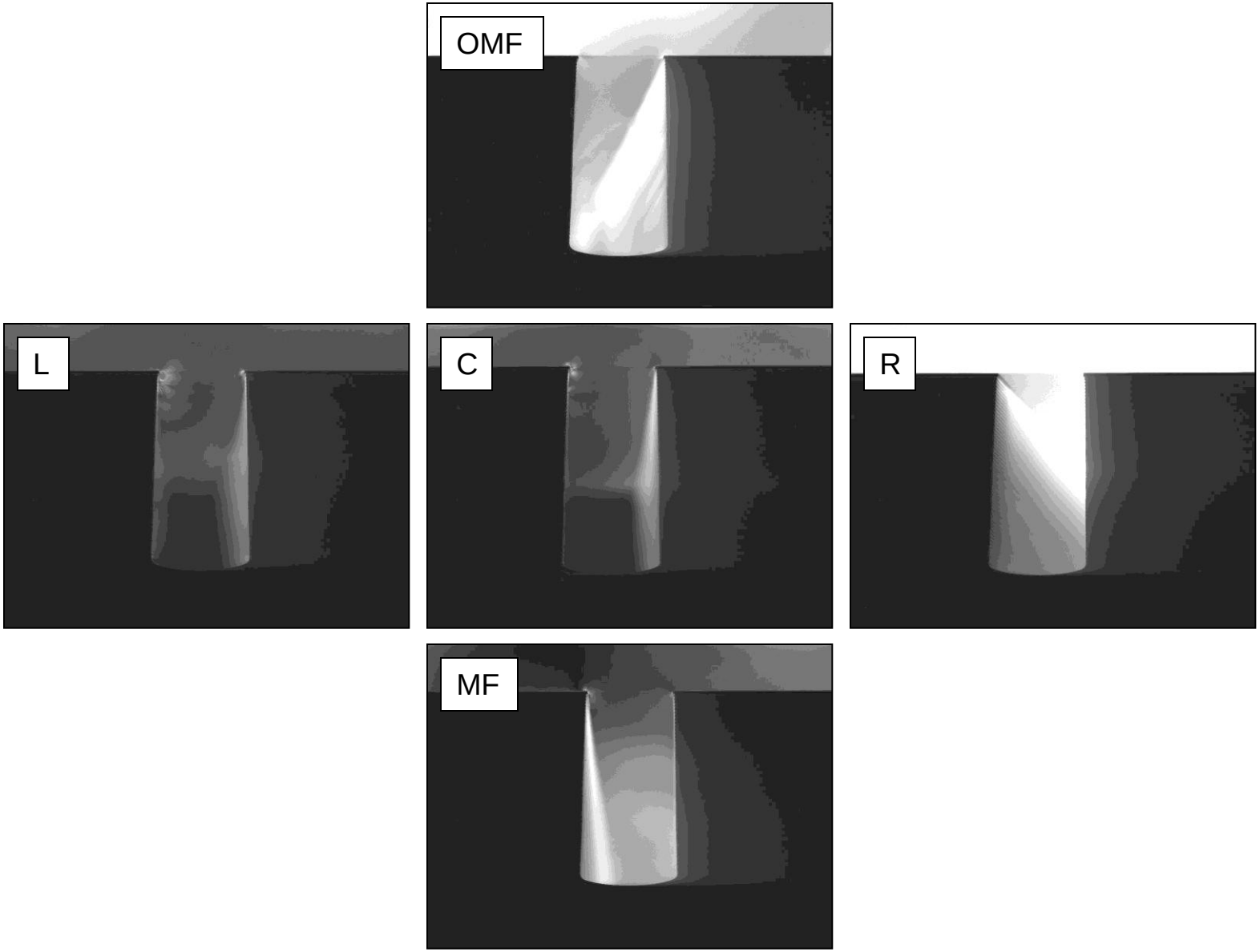
Process A - conditions

Step1 Dep – Etch (15s stab)	Etch	Dep
Gas Flow (sccm)	SF6 350 (1.5s) 550	C4F8 200
Cycle time (secs)	7.0	4.0
Pressure (mT)	25 (1.5s) 90>>150	25
APC angle (%)	7.88 >> 6.51	11.9
Coil power (w)	2800	2000
HF Platen power (w)	120>>140 (1.5s) 45	0
HF Platen M/U	Auto	Auto
Matching (Forward/ Load)	L/ 31 & T/ 55	-
Solenoids (A)	Off	Off
Time	2:01	

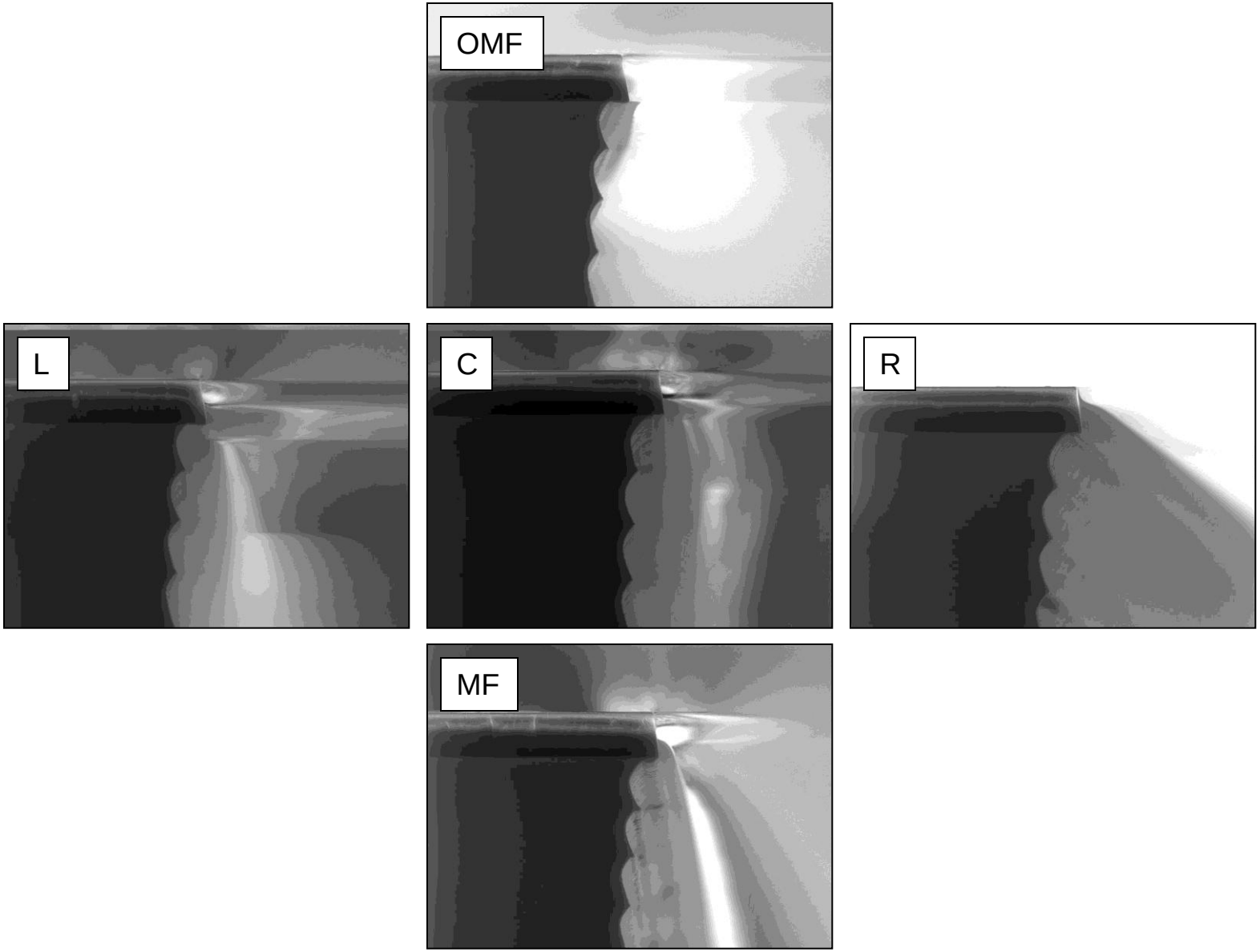
Step 2 Dep – Etch (No stab)	Etch	Dep
Gas Flow (sccm)	SF6 350 (1.5s) 550	C4F8 200
Cycle time (secs)	7.0	4.0
Pressure (mT)	25 (1.5s) 150	25
Coil power (w)	2800	2000
HF Platen power (w)	140 (1.5s) 45	0
HF Platen M/U	Auto	Auto
Solenoids (A)	Off	Off
Time	8:04	

Hardware configuration	Short funnel, with baffle & 5mm spacers
APC Gain	7.5 (default)
Platen Temperature	20
Process Time	10:05 mm:ss
Total cycles	55
HBC	10T

Process A – ‘Main’ SEM images (wafer 2, R#3)



Process A – ‘top’ SEM images (wafer 2, R#3)



Process A data – Wafer repeatability

- The data was collected using cross sectional analysis on an FE SEM at Danchip DTU.
- The wafer was cleaved to allow analysis of the following sites Centre, MF, OMF, Left & Right (with 5mm edge exclusion).

	Spec	Wafer 1	Wafer 2	Avg
Date & run no.		14th April, R#2	14th April, R#3	
STS datalog		16:24	19:20	
Depth (µm)	150	188.3	189.9	189.1
ER (µm/min)	>15	18.8	18.99	18.9
Mask Undercut (µm)	<1.5	0.622-1.198	0.551-0.886	0.840
Scallops (nm)	<800	718-790	551-742	718
Uniformity (±%)	<3.5	3.5	2.6	3.0
Selectivity (mask)	>150	252-300	241-367	310
Profile [º]	91 +/- 1	90.9-91.4	91.0-91.3	91.1

The wafer to wafer repeatability specification of < 4 % has been achieved with the result being 0.43 %. All other specifications for this process have been met.

Process B

30µm Via

(STS 150mm wafers)

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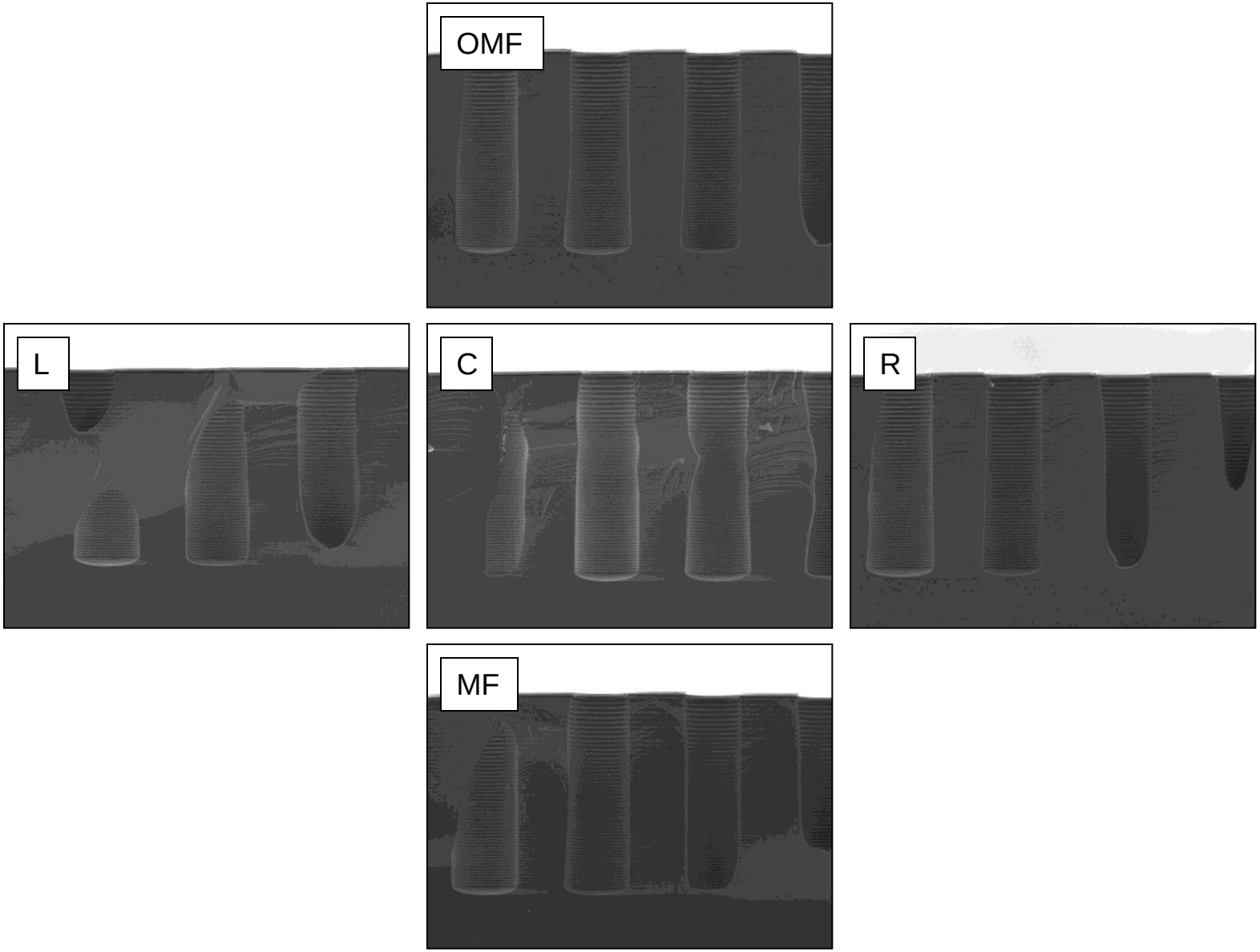
Process B – conditions

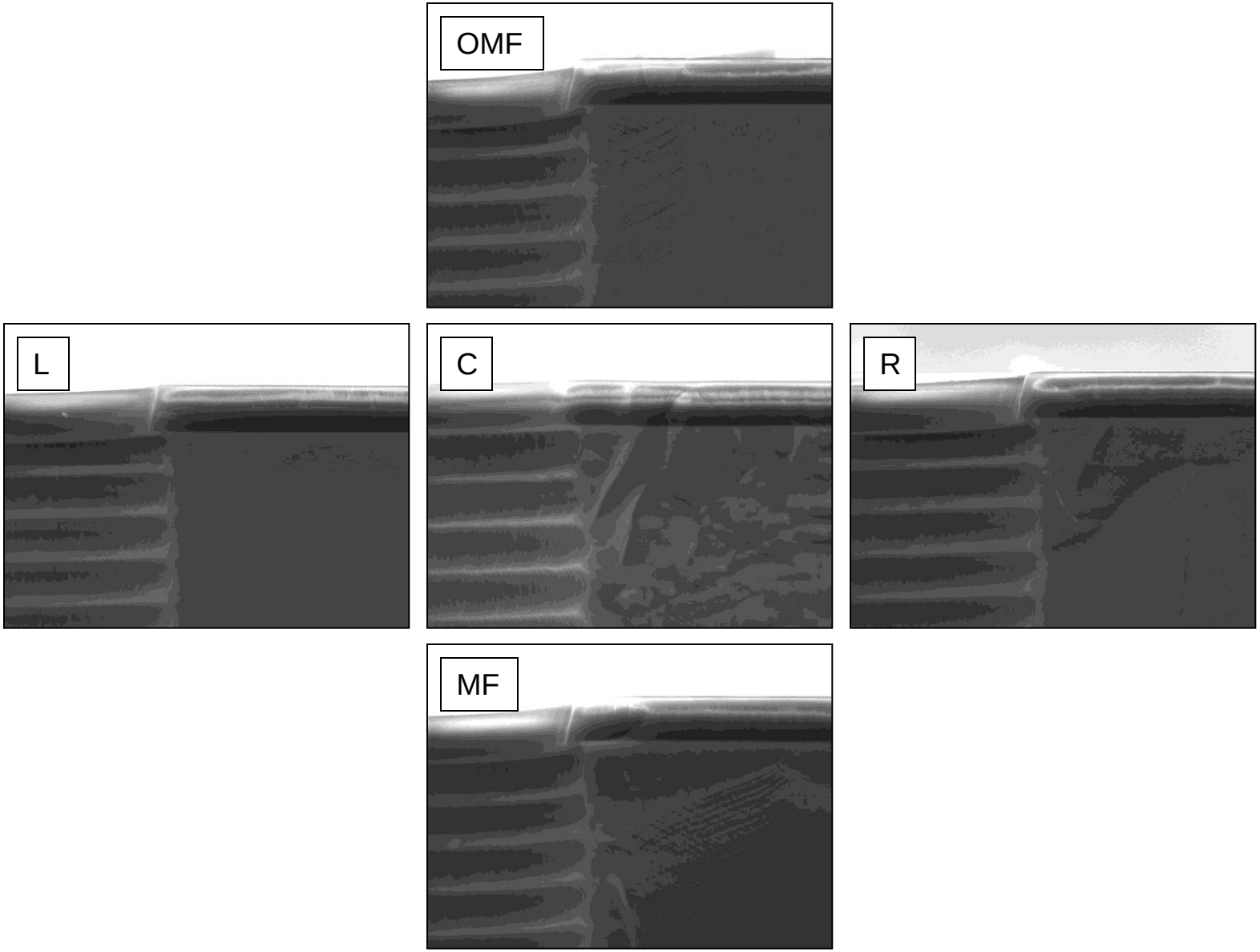
Main Etch (D→E)	Etch	Dep
Gas Flow (sccm)	SF6 350 + O2 35	C4F8 200
Cycle time (secs)	7.0	4.0
Pressure (mT)	20 (1.5s) 100	25
APC angle (%)	6.91	12.1
Coil power (w)	2800	2000
HF Platen power (w)	130 (1.5s) 40	0
Platen M/U	Auto	Auto
Solenoids (A)	Off	Off

Hardware configuration	Short funnel, with baffle & 5mm spacers, 10T HBC
APC Gain	7.5 (default)
Platen Temperature	10
Process Time	10:05 mm:ss
Total cycles	55

Process B – 'Main' SEM images (wafer 2, R#5)



Process B – 'top' SEM images (wafer 2, R#5)



Process B data – Wafer repeatability

- The data was collected using cross sectional analysis on a FE SEM at Danchip, DTU.
- The wafer was cleaved to allow analysis of the following sites Centre, MF, OMF, Left & Right (with 5mm edge exclusion).

Etch Characteristic	Spec	Wafer 1	Wafer 2	Avg
Date & run no.		15th April, R#4	15th April, R#5	
STS datalog		11:32	13:40	
Depth (µm)	100	107	106	107
ER (µm/min)	>10	10.7	10.5	10.7
Mask Undercut (µm)	<1.5	0.675-1.11	0.651-1.037	0.888
Scallops (nm)	<800	651-772	651-747	685
Uniformity (±%)	<3.5	2.38	3.11	2.7
Selectivity (mask)	>100	174-265	142-166	183
Profile [º]	91 +/- 1	90.5-91.2	90.3-91.1	90.7

The wafer to wafer repeatability specification of < 4 % has been achieved with the result being 0.47 %. All other specifications for this process have been met.

Process C

'Nano etch' (sub micron posts)

(Danchip 100mm wafers)

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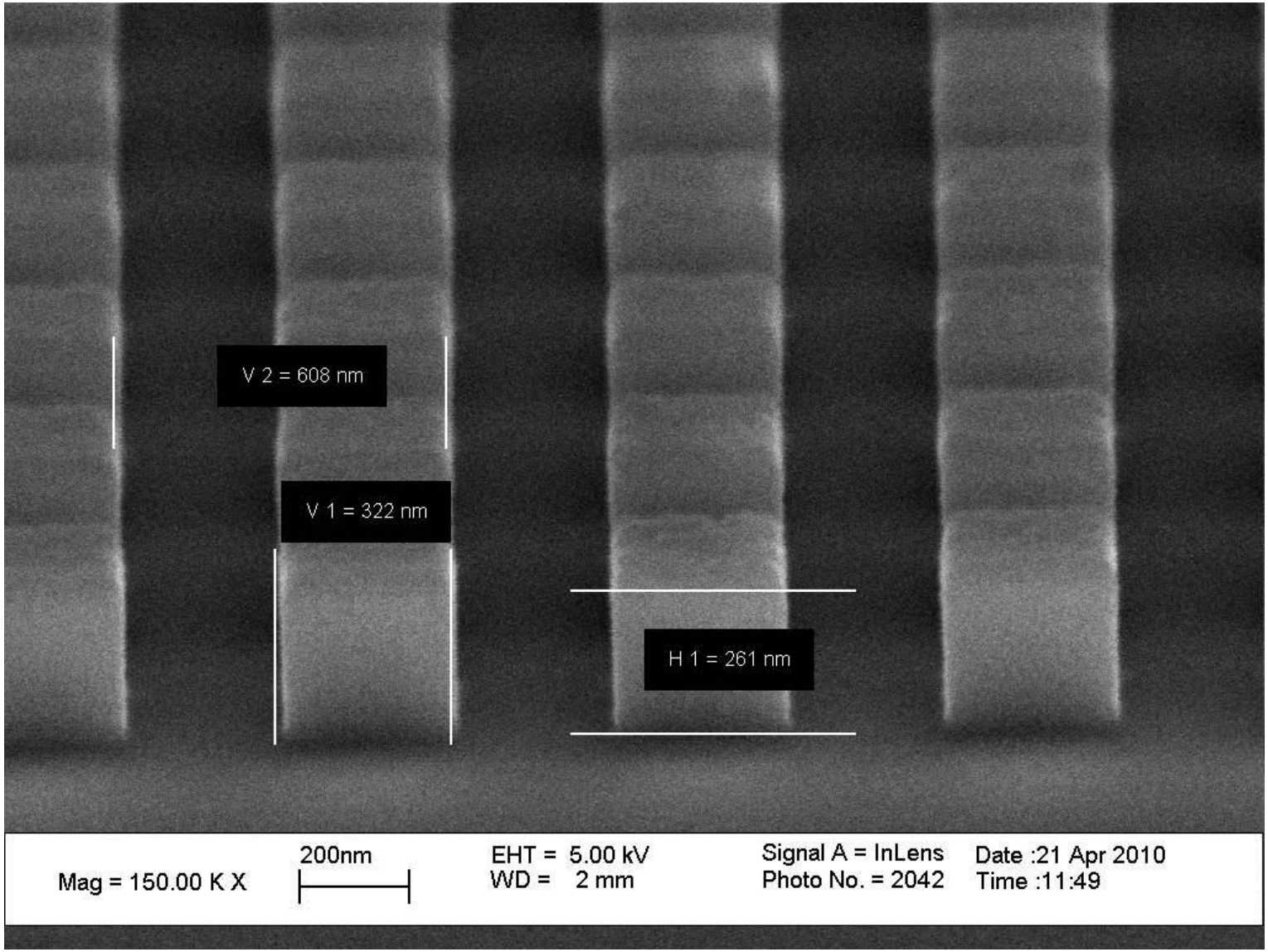
Process C – Final conditions

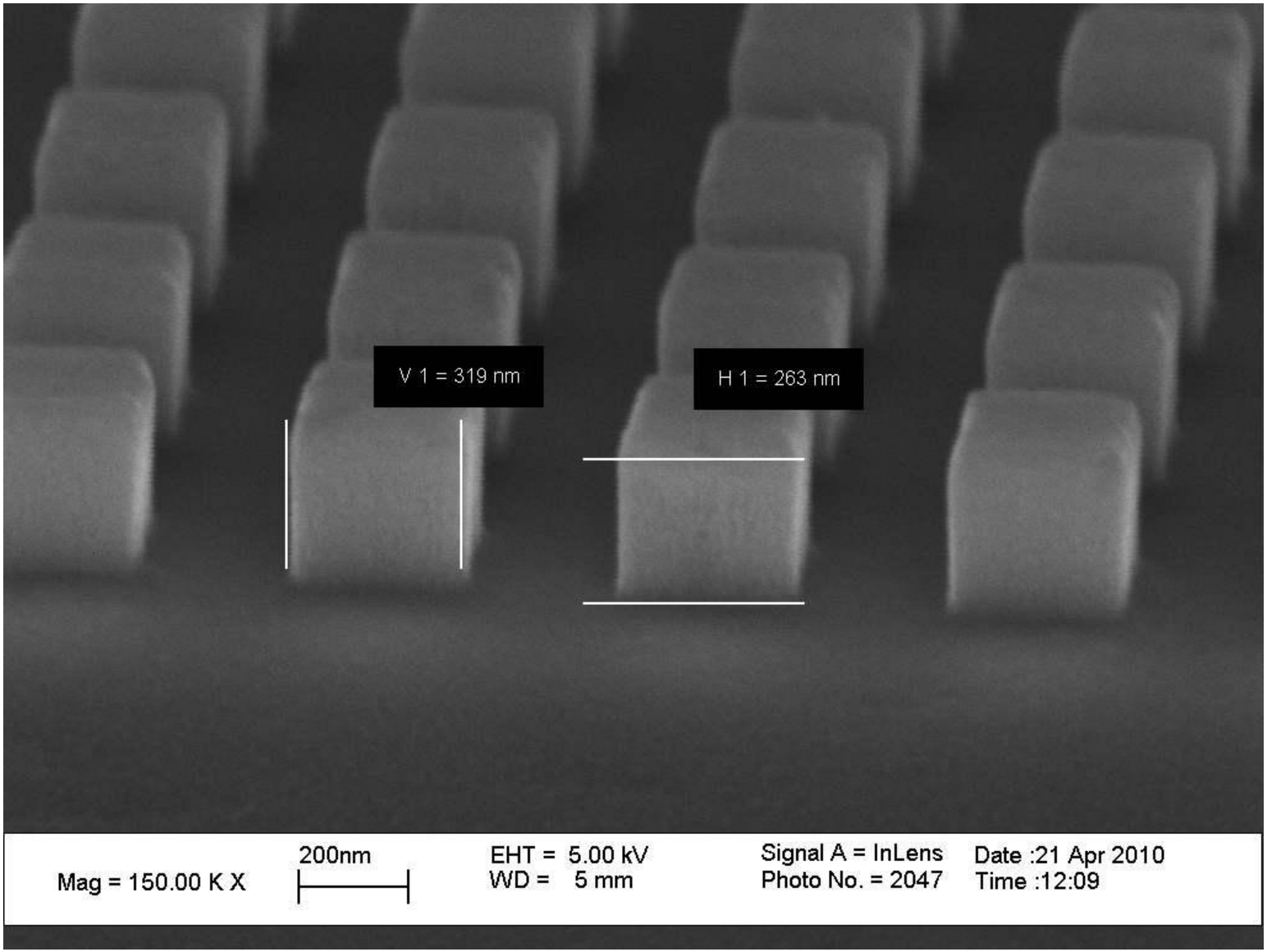
	Etch
Gas Flow (sccm)	SF6 38 + C4F8 70
Pressure (mT)	4
APC angle (%)	33.2
Coil power (w)	450
Matching (Forward/ Load)	L/ 33 & T/ 43
HF Platen power (w)	100
Matching (Forward/ Load)	L/ 49 & T/ 53
Solenoids (A)	Off
Time	01:30

Hardware configuration	150mm Long funnel, with baffle & 100mm spacers
APC Gain	7.5 (default)
Platen Temperature	10 C
Process Time	01:30 mm:ss

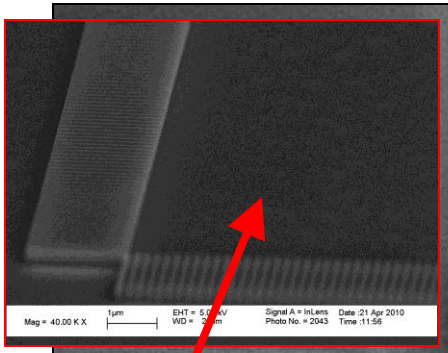
Process C – Images (R#12) – 300nm pillars - Centre



Process C – Images (R#12) – 300nm pillars – Edge (right)

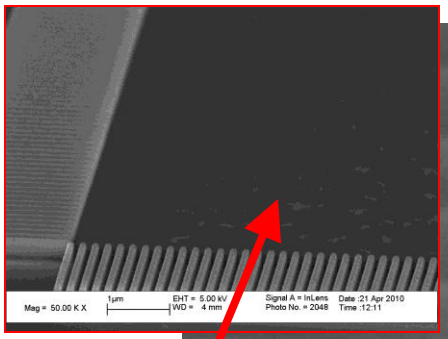


Process C – Images (R#12) – <300nm pillars - Centre



The smallest features (30nm pillars) did not survive lithography.

Process C – Images (R#12) – <300nm pillars – Edge (right)



The smallest features (30nm pillars) did not survive lithography.

H 1 = 283 nm

V 1 = 81 nm

50nm pillars

Mag = 200.00 K X

200nm

EHT = 5.00 kV
WD = 5 mm

Signal A = InLens
Photo No. = 2050

Date :21 Apr 2010
Time :12:16

Process C - etch summary

- The data was collected using cross sectional analysis on a FE SEM at Danchip, DTU.
- 300nm pillars were inspected centre and edge.
- The smallest features resolved by the lithography (50nm pillars) were also inspected.
- The 30nm pillars were not successfully formed by lithography.
- Run #12 has etched the wafer, this can be seen from the SEM images of the ~300nm dots. The depth of these features is *ca* 260nm (not including the mask).
- The Si etch rate is ~170nm/min.
- The cross wafer uniformity is good (< 1%, n=2) & the profile vertical.

Process D

Micro stamp etch (4µm trenches)

(Danchip 100mm wafers)

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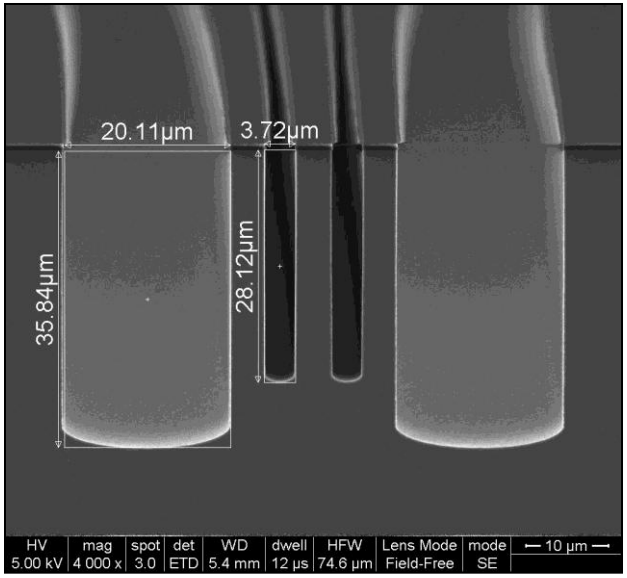
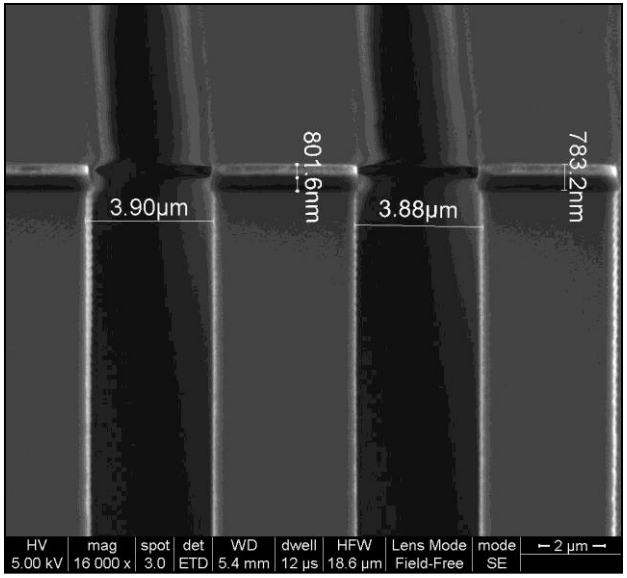
Process D – Final conditions

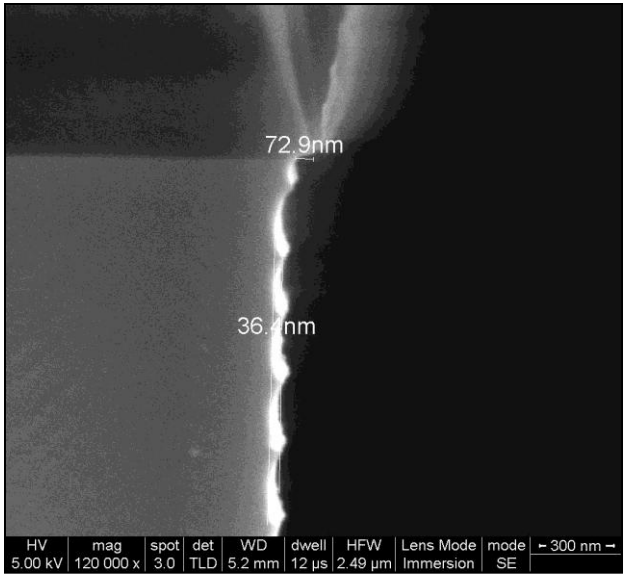
Main Etch	Etch	Dep
Gas Flow (sccm)	SF6 275 + O2 5	C4F8 150
Cycle time (secs)	2.4	2.0
Pressure (mT)	26	20
APC angle (%)	12.4	10.3
Coil power (w)	2500	2000
HF Platen power (w)	35	0
Matching (Forward/ Load)	L/ 40 & T/ 51	-
Solenoids (A)	Off	Off

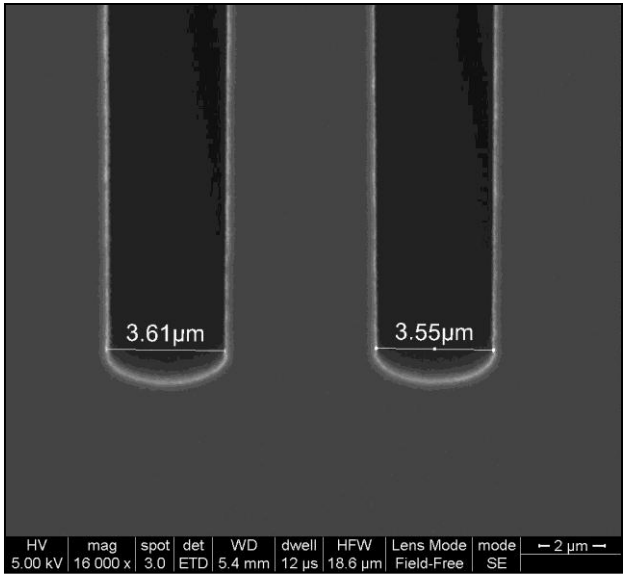
Hardware configuration	150mm Long funnel, with baffle & 100mm spacers
APC Gain	7.5 (default)
Platen Temperature	0
Process Time	08:04 mm:ss
Total cycles	110

Process D – NE images (run 6)

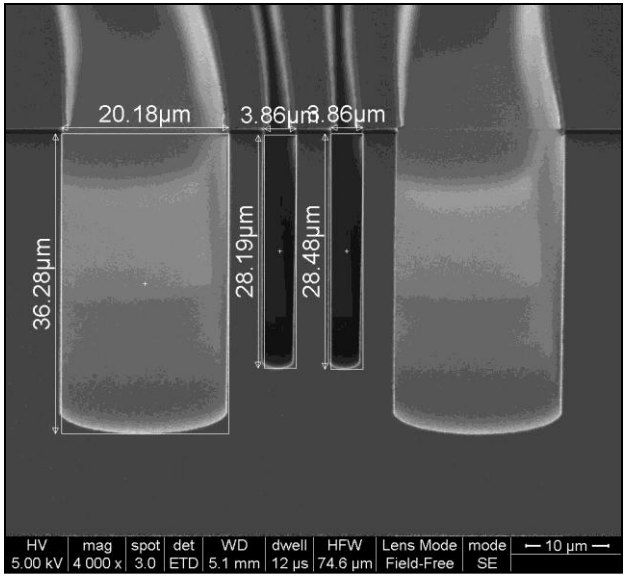


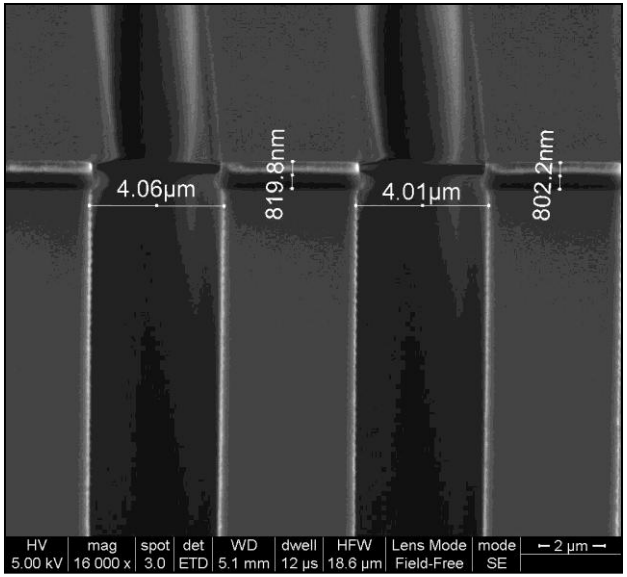


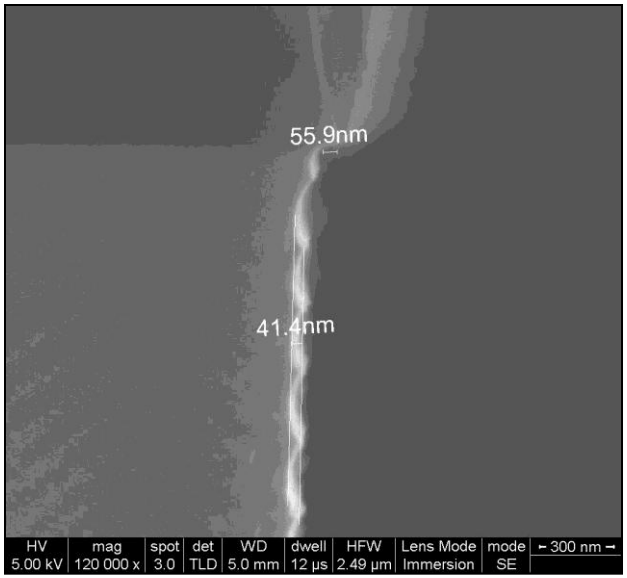


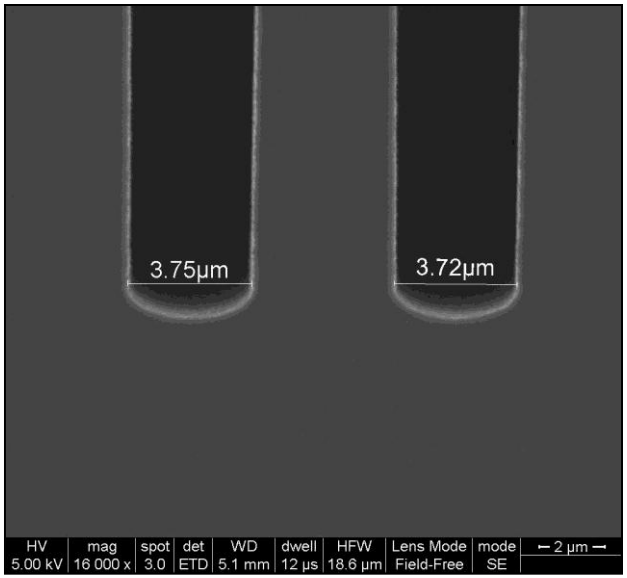


Process D – NW images (run 6)

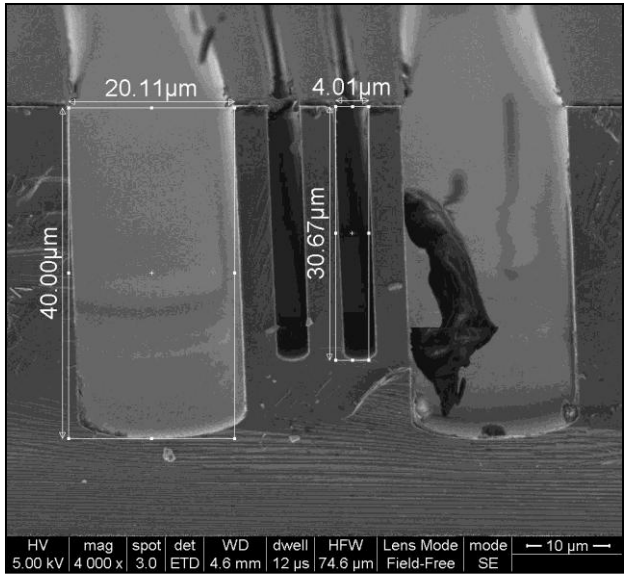


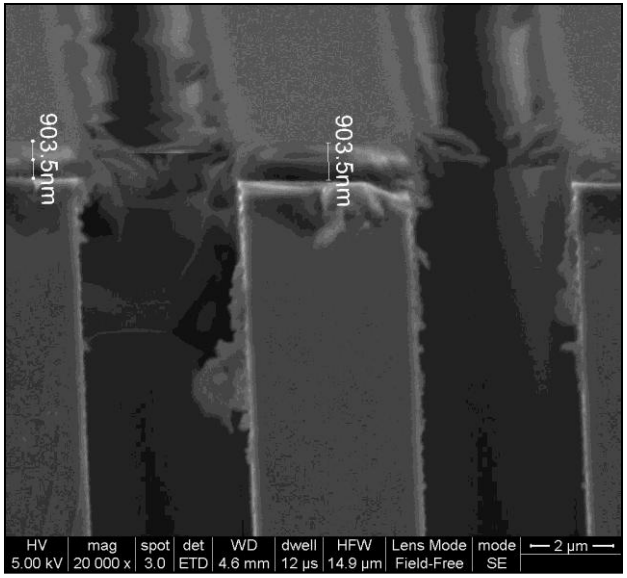


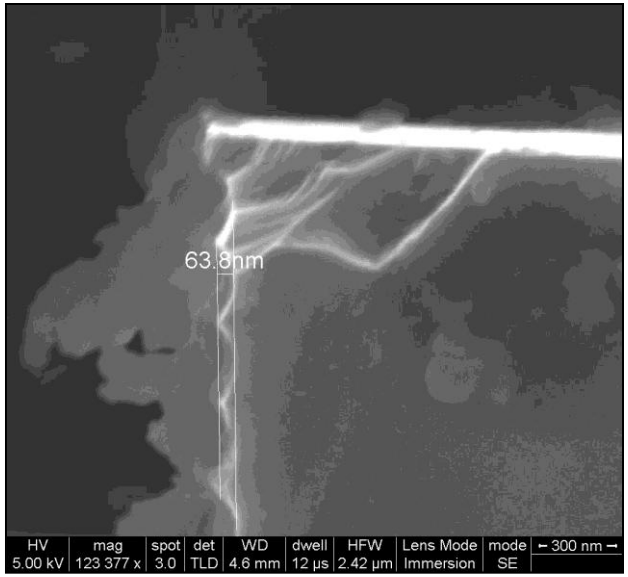


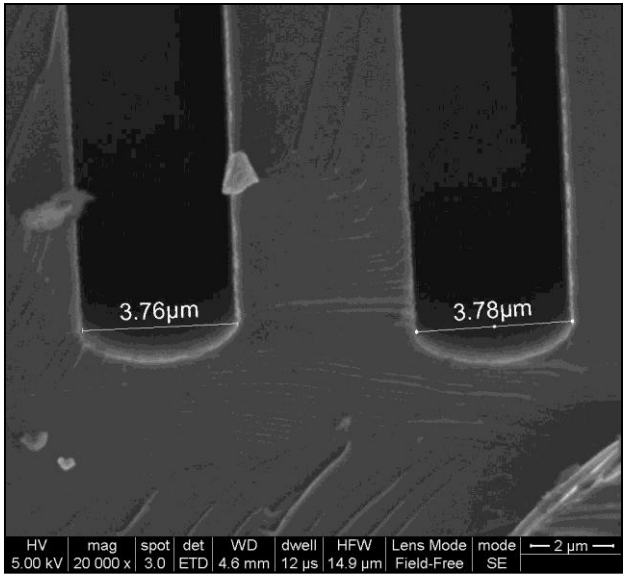


Process D – SE images (run 6)

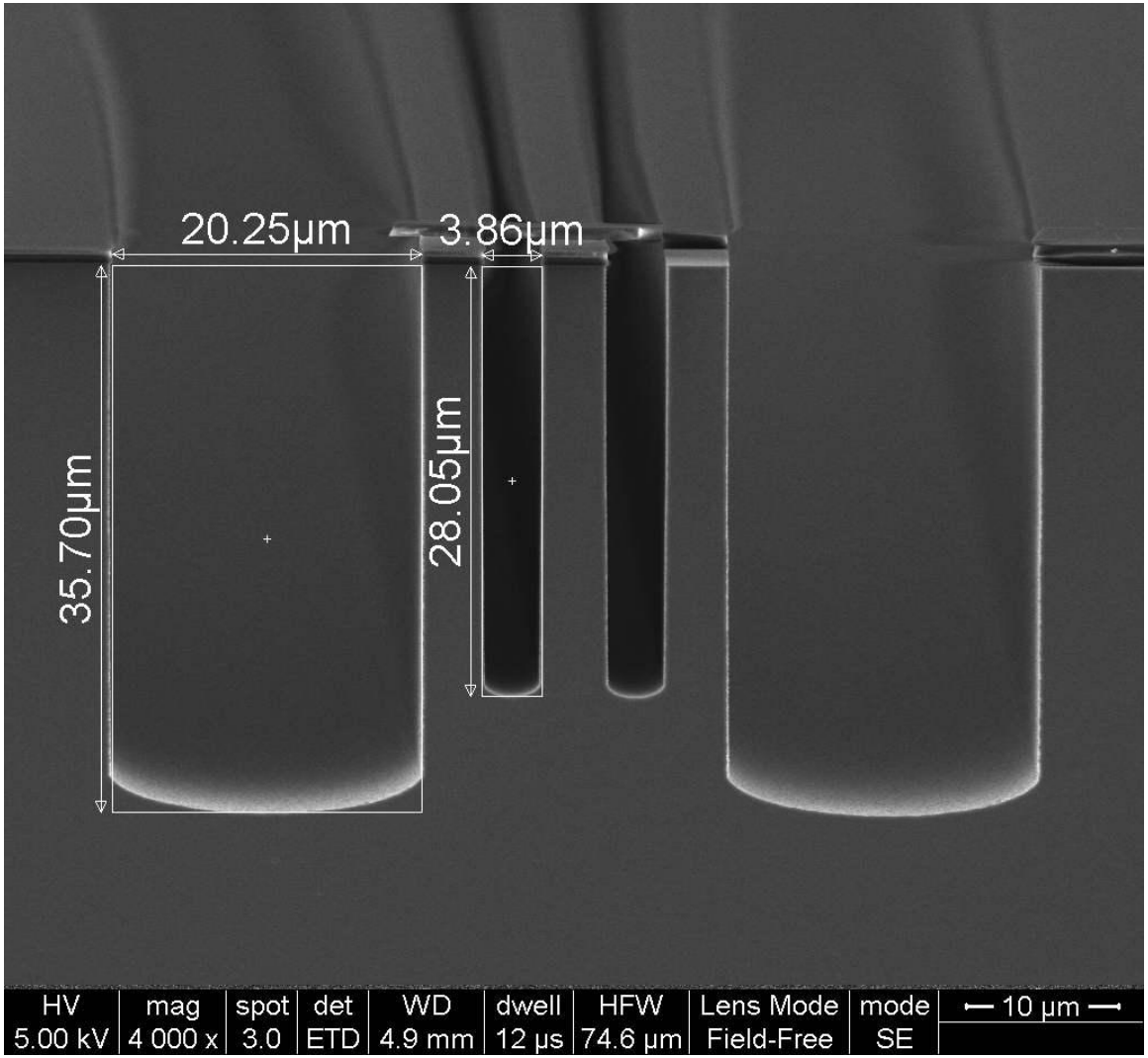


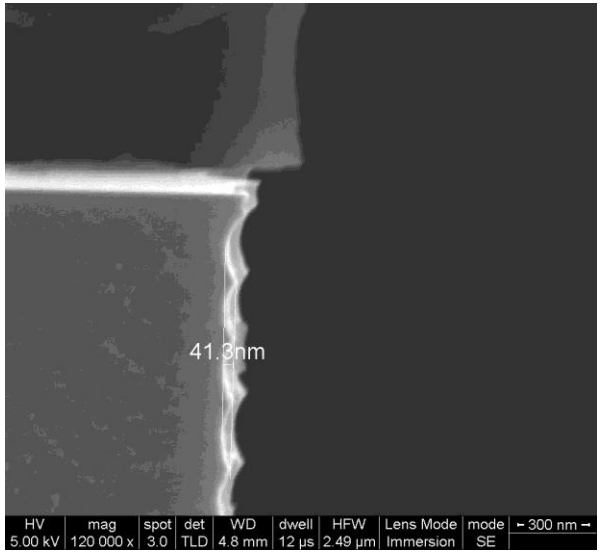


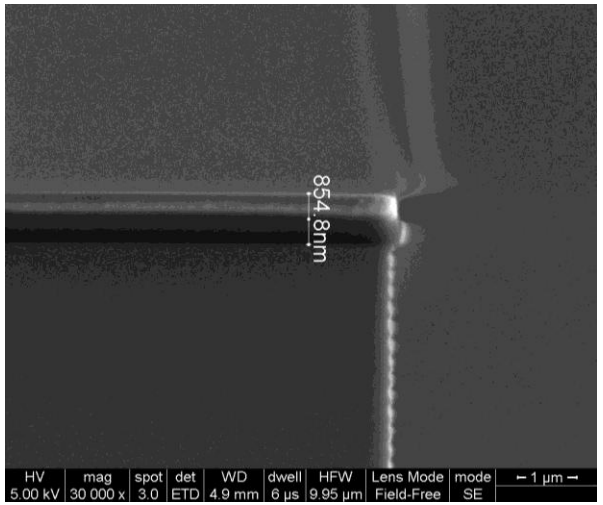




Process D – SW images (run 6)







Process D data – Data summary

- The data was collected using cross sectional analysis on a FE SEM at Danchip DTU.
- The wafer was cleaved to allow analysis of the following sites NE, NW, SE, & SW.

Etch Characteristic	Spec	Features of interest	Avg
Depth (µm)	20-30 (e-mail 25/11/09)	28.05 - 30.67	28.75
ER (µm/min)	NS	2.81 - 3.08	2.88
Mask Undercut (nm)	NS	56 – 73	65
Scallops (nm)	<30	36 - 64	46
Uniformity (±%)	<3.5	4.56* 0.25*	4.56* 0.25*
Selectivity (mask)	NS	42-67	50
Profile [°]	85 +/- 5	89.7 - 89.8	89.7

*The features of interest are not positioned in exactly the same area at the 4 measured sites. At the SE site the features are nearer the edge (2.5mm from edge) of the wafer resulting in a greater etch depth and more tilting. The impact on uniformity can be seen in this table, the upper value of 4.56% has the SE point included and the lower value of 0.25% does not include the SE site.

FA MP0534 - Summary

- All processes have been successfully demonstrated during this Field Acceptance.
- Two applications have been demonstrated at 150mm using STS material and two applications at 100mm using Danchip material.
- The results show that process specification have been met on individual wafers across all for applications. In addition processes A and B have demonstrated good wafer to wafer repeatability.
- The tools Low Frequency SOI capability has been successfully demonstrated.

Demonstration of Low frequency (380kHz) SOI capability

40 & 50µm Trenches

(Danchip 100mm wafers)

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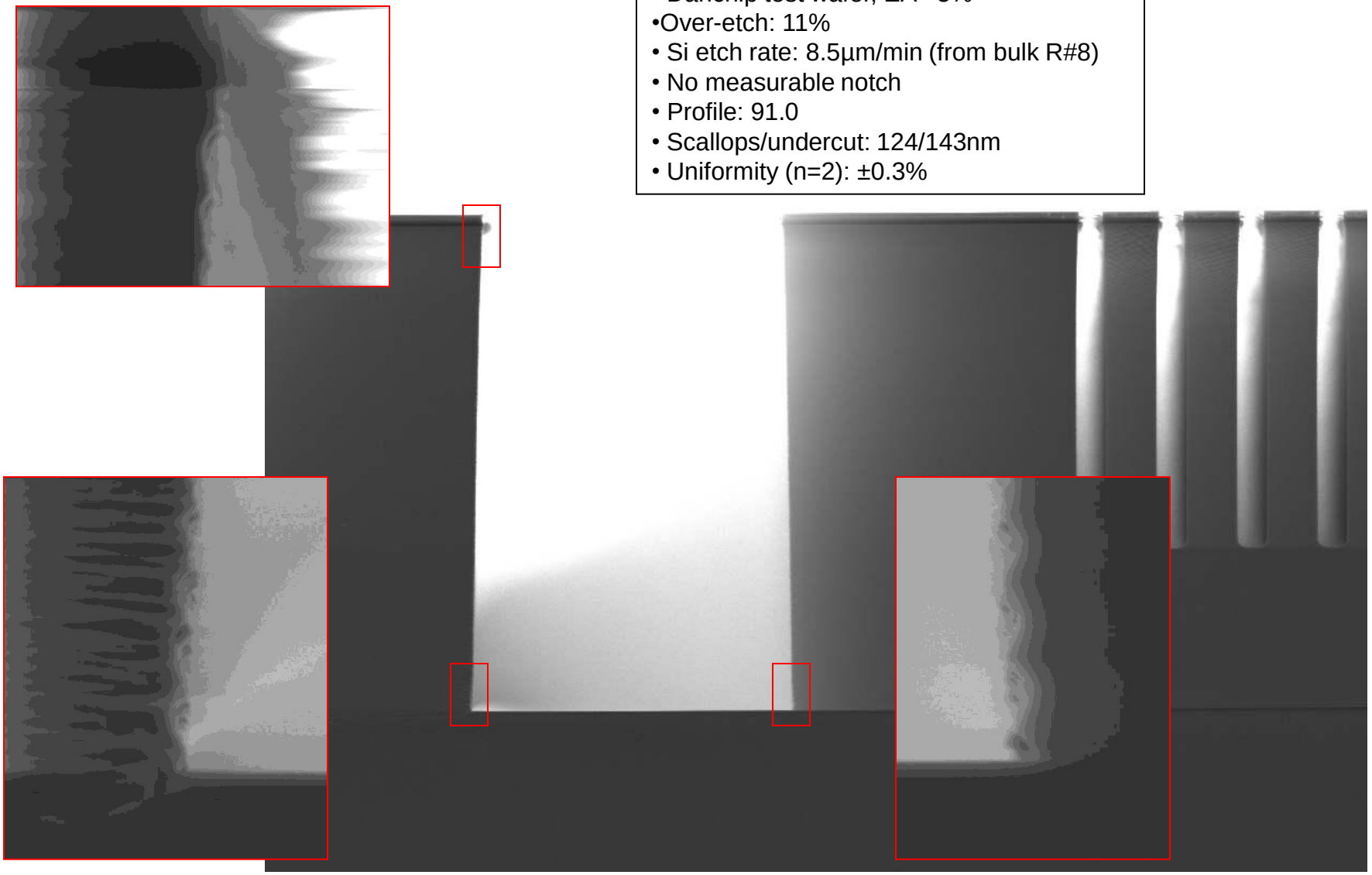
LF SOI Demonstration – process conditions

Main Etch	Etch	Dep
Gas Flow (sccm)	SF6 400 + O2 40	C4F8 250
Cycle time (secs)	3.0	2.0
Pressure (mT)	30	25
Coil power (w)	2800	2000
LF Platen power (w)	75	0
LF Platen Pulsing software set-up	0.025s, 75%	-
Platen Matching	Auto	Auto
Solenoids (A)	Off	Off

Hardware configuration	150mm Long funnel, with baffle & 100mm spacers
APC Gain	7.5 (default)
Platen Temperature	20 C
Process Time	8 min
Total cycles	96

LF SOI Demonstration - 40µm Trench, wafer edge (R#7)

- Danchip test wafer, EA ~5%
- Over-etch: 11%
- Si etch rate: 8.5µm/min (from bulk R#8)
- No measurable notch
- Profile: 91.0
- Scallops/undercut: 124/143nm
- Uniformity (n=2): ±0.3%



LF SOI Demonstration - 50µm Trench, Centre & edge (R#7)