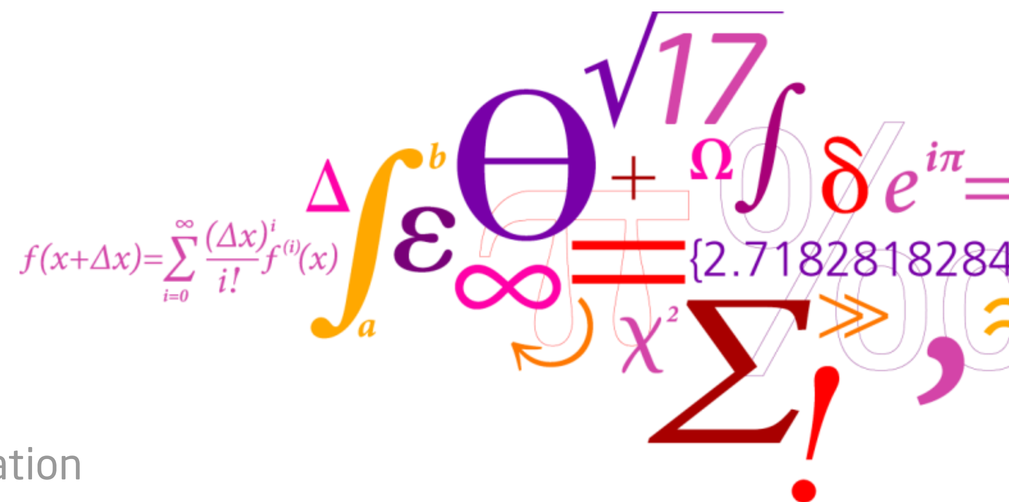
DTU Danchip

Tech Forum

Date: 5th February 2013

Time: 11 to 12

Place: Cafe, Building 347



DTU Danchip

National Center for Micro- and Nanofabrication

tech forum

Intensify dialog especially on a strategic level between Danchip and Danchip users

What does free of charge mean ?

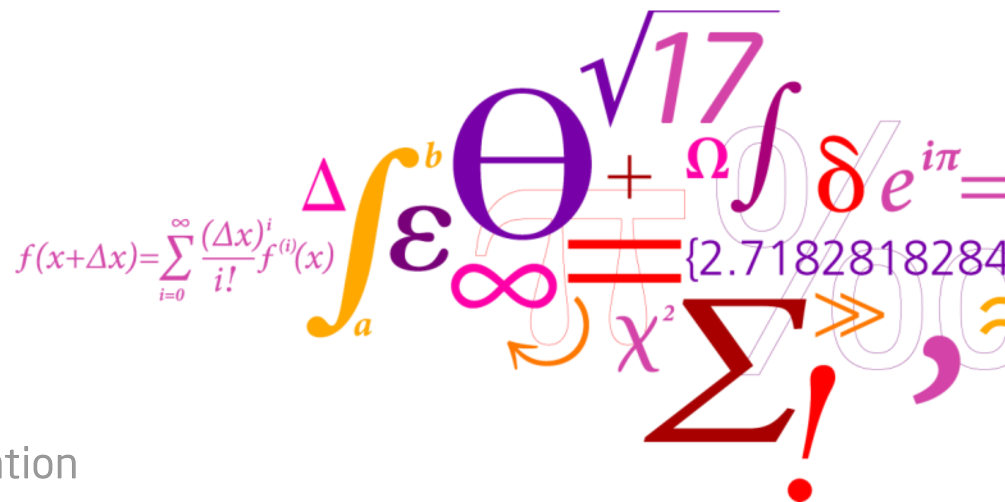
All (reasonable) cleanroom usage including

hourly rate of cleanroom fee and machine use…..

Not including explicit materials e.g. wafers,

thick noble metal layers,

masks etc



Pricing model strongly inspired by UC Berkely, Stanford, MIT

- Cleanroom admission (including suits, gloves, characterization equipment and basic tools which are easy to maintain)
- Floor space rent
- 3 equipment groups
  - Group A: tools that are cost efficient to maintain and use no/few low cost consumables
  - Group B: tools that are more costly to maintain and use considerable/costly consumables
  - Group C: complicated, advanced tools (one of a kind) that require expensive service contracts and have a very high cost of ownership

Actual pricing is calculated by DTU's financial analysis group based on the usage and capacity of the respective tools

Prices – external commercial users (UK90)

Service from Danchip	New price 2013	Present price 2012	Unit
Cleanroom access (below cap)[a)]	750	800	kr/h
Danchip assistance	1200	1200	kr/h
Cleanroom area	1600	2100	kr/m^2/mo
Category A tools	350	200-2000	kr/h
Category B tools	600	550-2000	kr/h
Category C tools	3500	4000	kr/h
Category F tools[b)]	0	0-275	kr/h

a) Cleanroom access above cap of 20 hours is 0 kr/h

b) Tools paid for by their booking (8.x, not SIMS, XPS) are of type F but charged as Category A when booked

c) Materials (e.g. Wafers, metals, masks) are charged at their cost price

Prices – external funded projects and users (UK95, other universities: UK10)

+ overhead

Service from Danchip	New price 2013	Present price 2012	
Cleanroom access (below cap)[a)]	333	800	kr/h
Danchip assistance	450	1200	kr/h
Cleanroom area	400	2100	kr/m²/mo
Category A tools	150	200-2000	kr/h
Category B tools	250	550-2000	kr/h
Category C tools	1500	4000	kr/h
Category F tools[b)]	0	0-275	kr/h

a) Cleanroom access above cap of 20 hours is 0 kr/h

b) Tools paid for by their booking (8.x, not SIMS, XPS) are of type F but charged as Category A when booked

c) Materials (e.g. Wafers, metals, masks) are charged at their cost price, Electronic invoicing system will be used if at all possible

Why tech forum?

dialog on a strategic level - enhance general communication

- information on new technologies, new possibilities at Danchip
- discuss possible future technologies at Danchip
- work together on securing funding for new tools
- talk about important general operational issues

today

Status laser, seed metallization

Status photolith e-beam and stepper

Thermal oxide

Coming technologies:

Status ellipsometer

Furnace multi purpose hydrogen anneal

ALD

Situation indicator

Stage	Description
Idea	
Users	Critical mass of users
Funds	How to pay for the tool?
Tender	Very precise description
Contract	The actual terms
FAT	Factory Acceptance Test
SAT	Site Acceptance Test
Manual	Simplified manual
Released	Out of the initial phase, put to use

3DMM Laser micromachining tool 7.013

Expected ready for training ~May 2013

Demo samples

Samples made by direct laserwriting in a nickel shim

Pattern with pyramids with a base of 100 µm and 200 µm

Shim thickness 630 µm, cutout time 10 min

Polymer: Topas 8007S-04, form time 61 s

Sputtering of Ti/W in Wordentec for Ni plating seed layer

- **Two standard TiW sputtering processes were evaluated:**

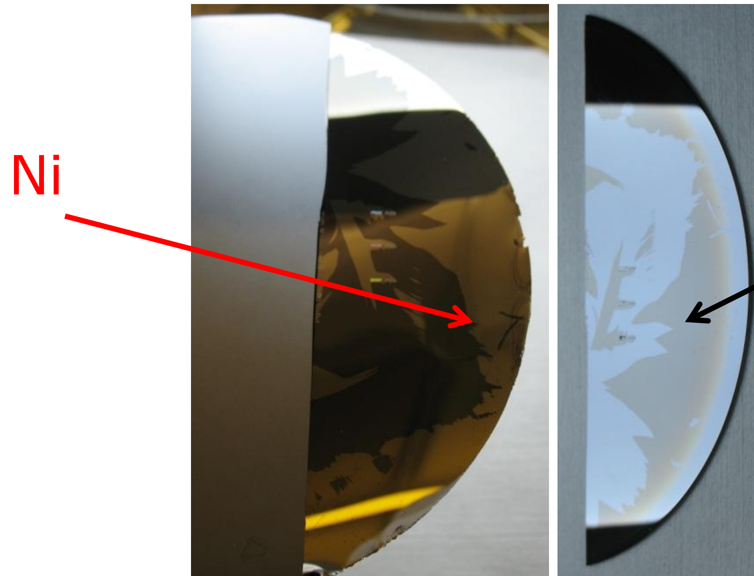
	Process 1	Process 2
Pressure	0,05 mbar	0,001 mbar
Power	250W	150W
Nominal rate	2,4 Å/s	1,0 Å/s
Process time	10min	16min40sec
Expected thickness	144 nm	100 nm

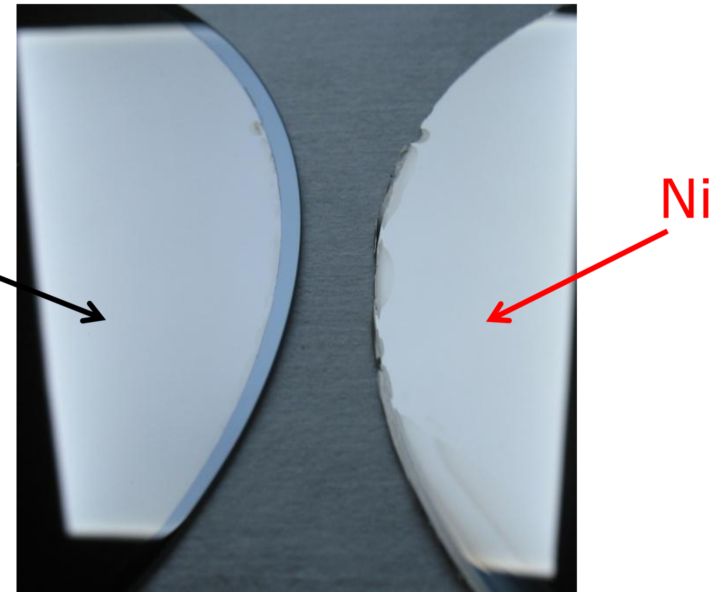
- Test procedure
  - ✓ Seed layer was deposited on blank 100 mm silicon wafers
  - ✓ Samples were electroplated at I_{max} = 4,50 A and Q = 5,8 Ah resulting in 100 µm thickness nickel samples
  - ✓ Samples were separated gently by hand

Sputtering of Ti/W in Wordentec

Process 1

Process 2





Conclusion

- TiW shows good compatibility (chemically and electrically) with the nickel plating process
- Process 1 (0,05 mbar): Poor seed layer adhesion. Seed layer adheres partly to Si and partly to Ni after separation
- Process 2 (0,001 mbar): Excellent seed layer adhesion to Si. All seed layer remains on Si after separation.

DTU

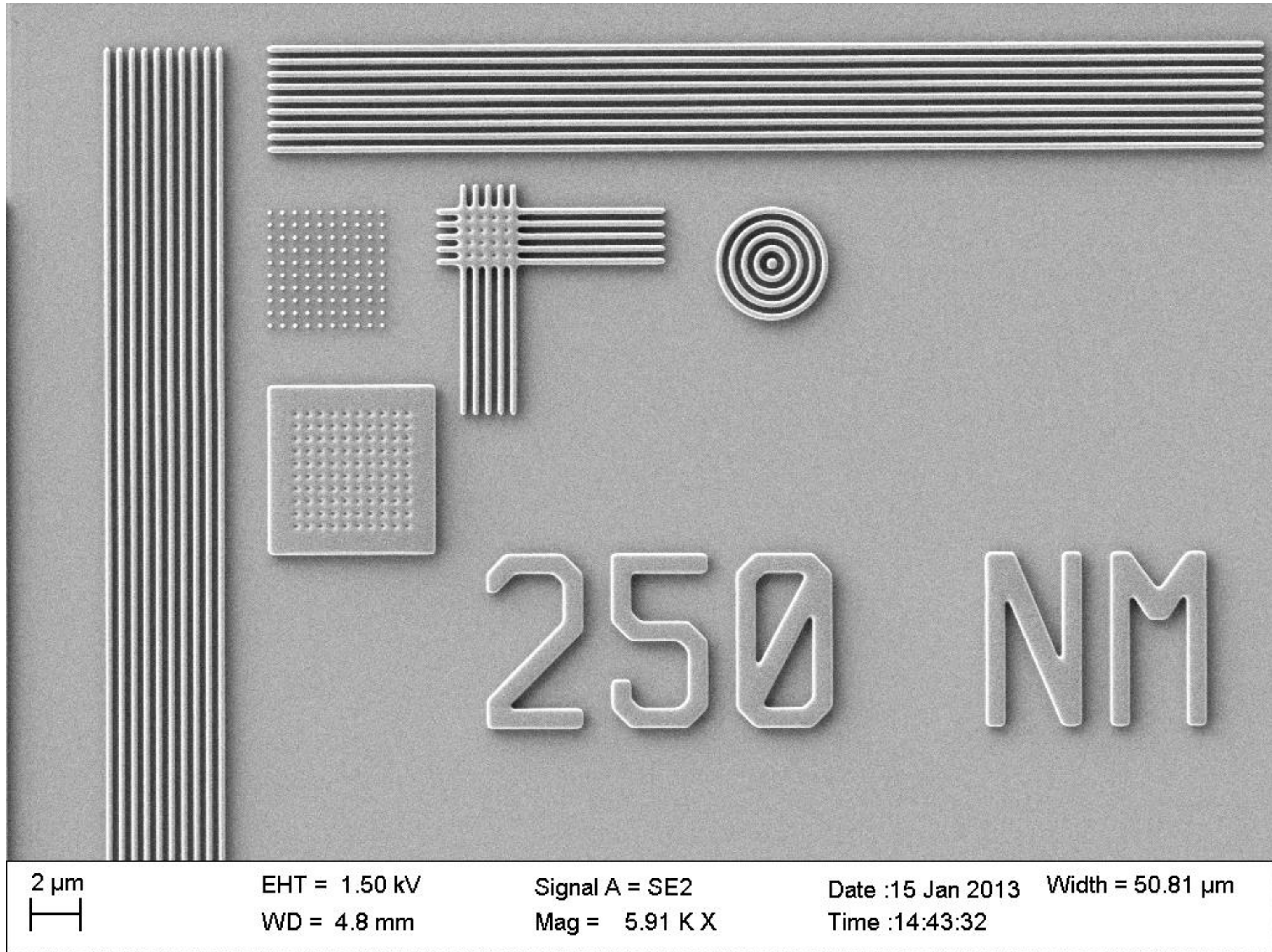
New Spin Track

- Installation ongoing
- Facilities connected
- Wafer handling optimised
- Set to 4”
- Wet process optimisation will start this week

DUV Process Status

- 400 nm positive process established
- 1 µm positive process established
- 400 nm negative process established
- 6” is standard
- 4” can be processed in trays
- 8” possible: chuck change needed
- 400 nm positive process
  - Canon minimum guaranteed feature size 250 nm
  - Super illumination mode: down to 160 nm (only lines/spaces)
- Stitching < 40 nm
- Alignment < 50 nm

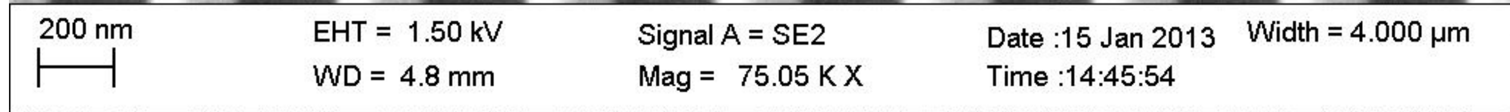
Positive process – 400 nm resist thickness



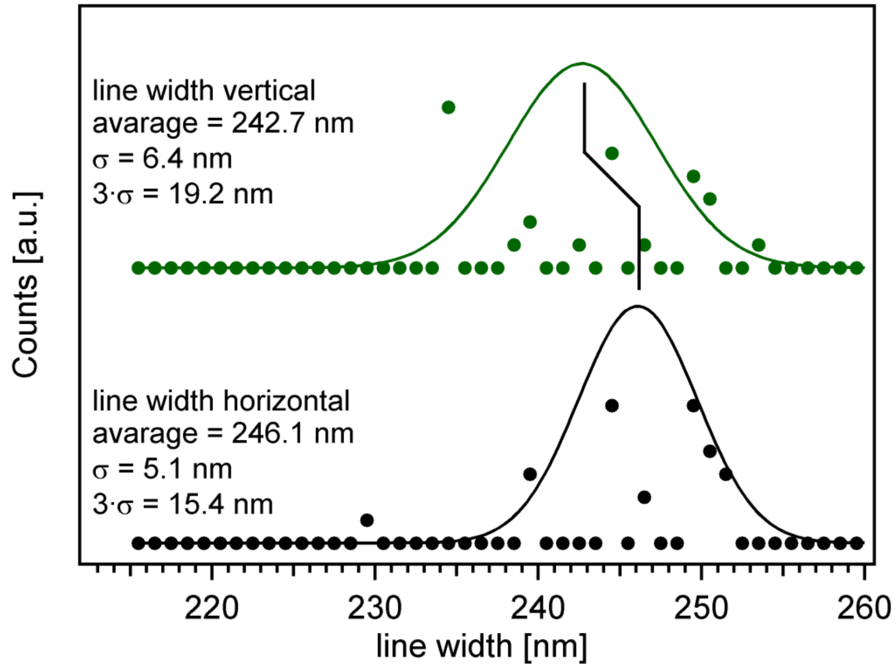
Positive 250 nm lines/spaces

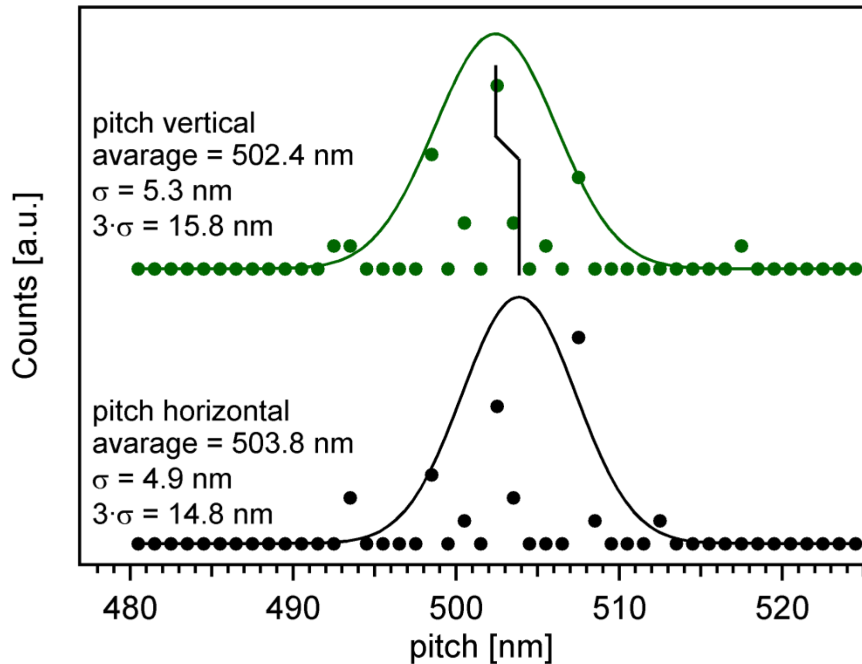
V 1 = 246.1 nm

V 2 = 500.0 nm



6" wafers: 250 nm l/s stat. (wafers 215, 218, 229, 1261, 6811)





Illumination mode

Changing partial coherence factor σ

$$\sigma = \frac{\sin(\theta_{max})}{Na} = \frac{\text{source diameter}}{\text{lense diameter}}$$

θ: half angle of the illumination cone on the reticle from the source

$\sigma = 0$ coherent light

$\sigma = \infty$ incoherent light

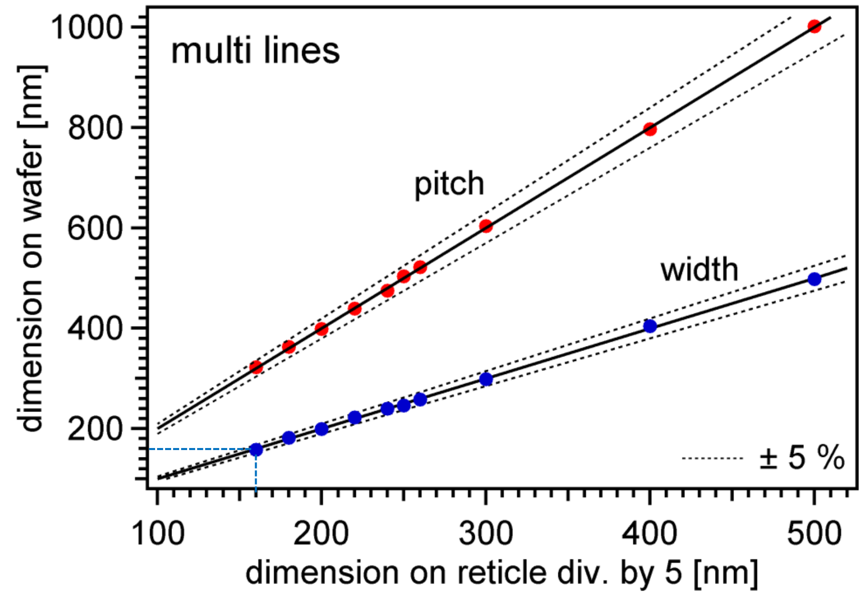
	σ	NA
1	0,65	0,6
2	0,5	0,6
3	0,4	0,6
6	SIA2	0,6

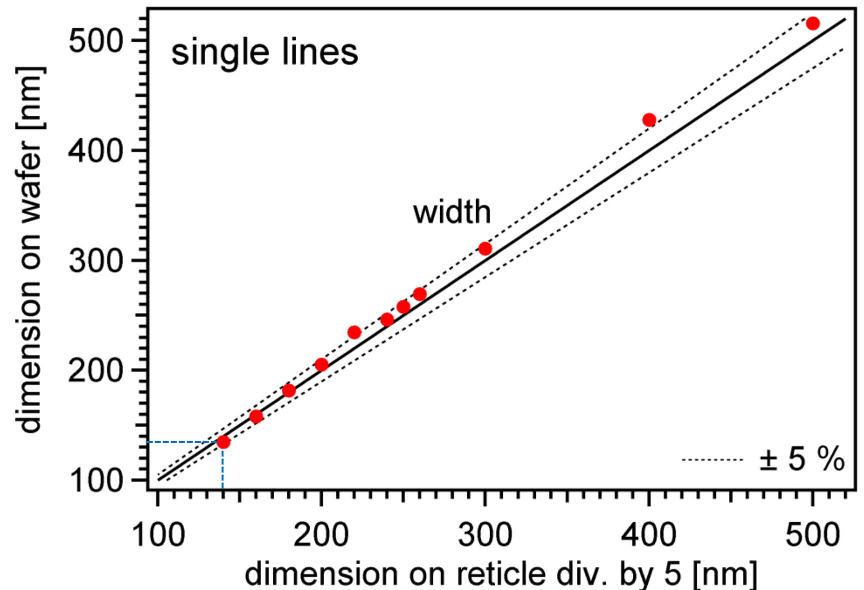
Resolution

Multi lines: 160nm

Single lines: 140 nm

Stepper performance in super illumination mode (SIA2)
- verticle lines -





Super illumination mode SIA2:

140 nm

2 µm | EHT = 1.50 kV | WD = 3.9 mm | Signal A = SE2 | Mag = 11.67 K X | Date :13 Sep 2012 | Time :14:27:07 | Width = 25.73 µm

140 nm

134.8 nm

200 nm | EHT = 1.50 kV | WD = 3.9 mm | Signal A = SE2 | Mag = 50.03 K X | Date :13 Sep 2012 | Time :14:21:02 | Width = 6.000 µm

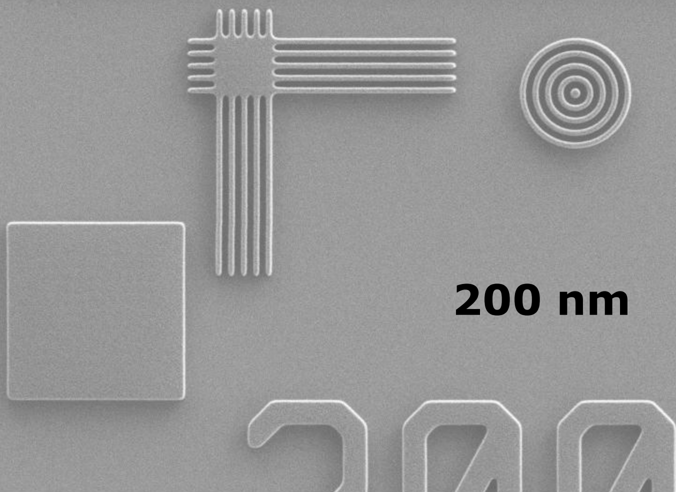
160 nm

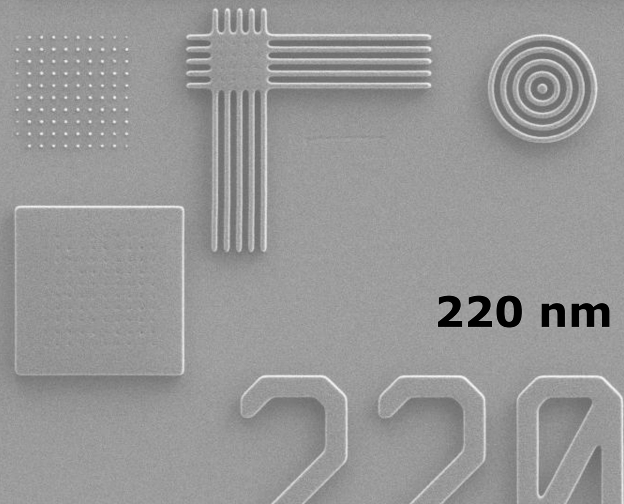
2 µm | EHT = 1.50 kV | WD = 3.9 mm | Signal A = SE2 | Mag = 12.55 K X | Date :13 Sep 2012 | Time :14:25:54 | Width = 23.92 µm

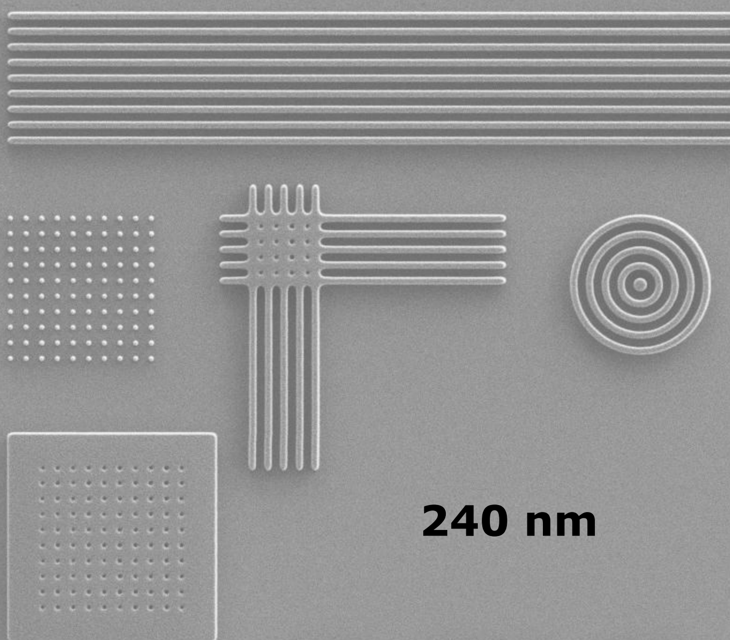
180 nm

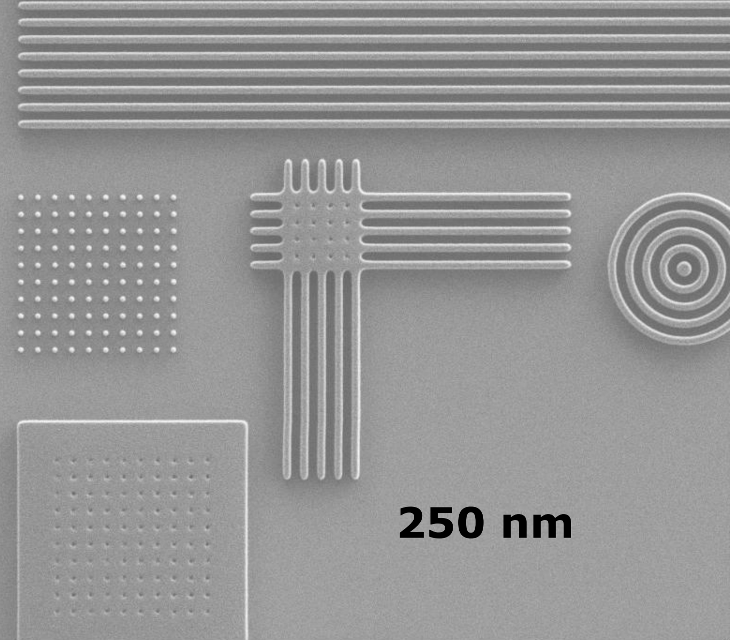
2 µm | EHT = 1.50 kV | WD = 3.9 mm | Signal A = SE2 | Mag = 12.55 K X | Date :13 Sep 2012 | Time :14:24:29 | Width = 23.92 µm

Super illumination mode SIA2:





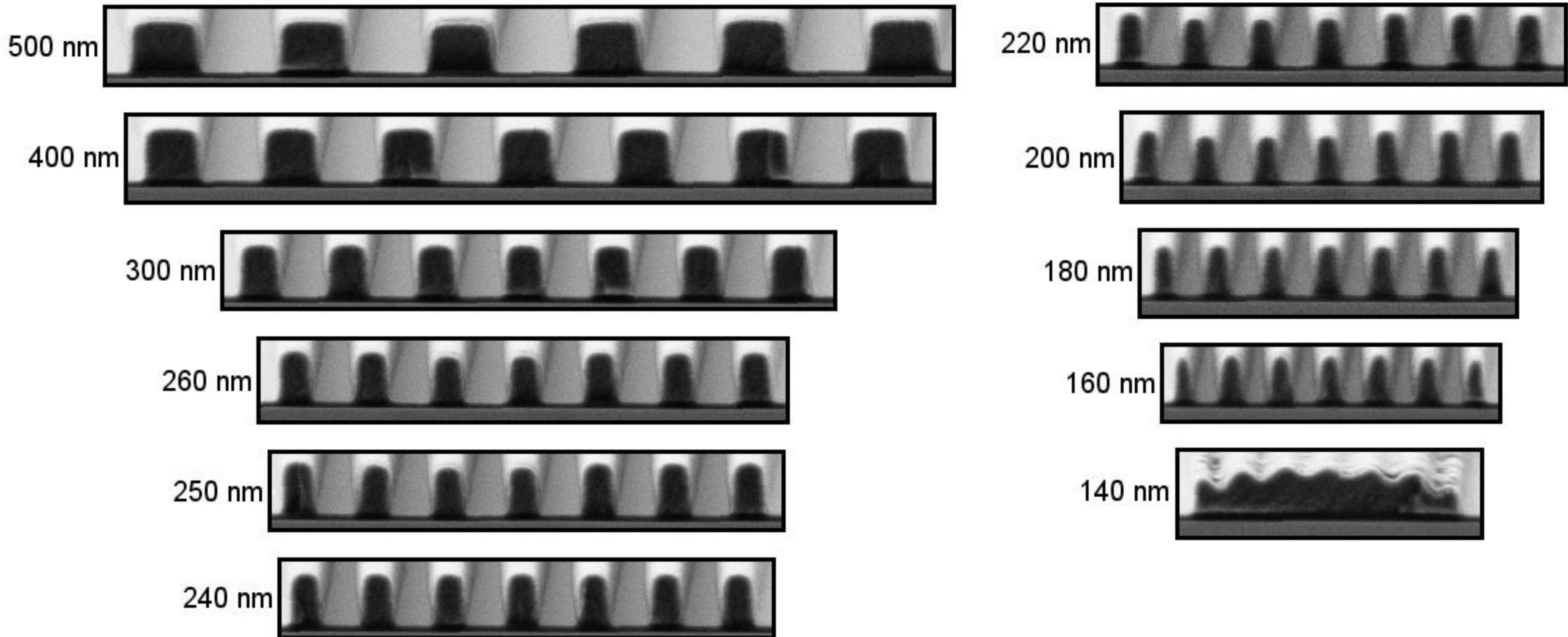




Resolution at 220 J/m^2

SEM profile:

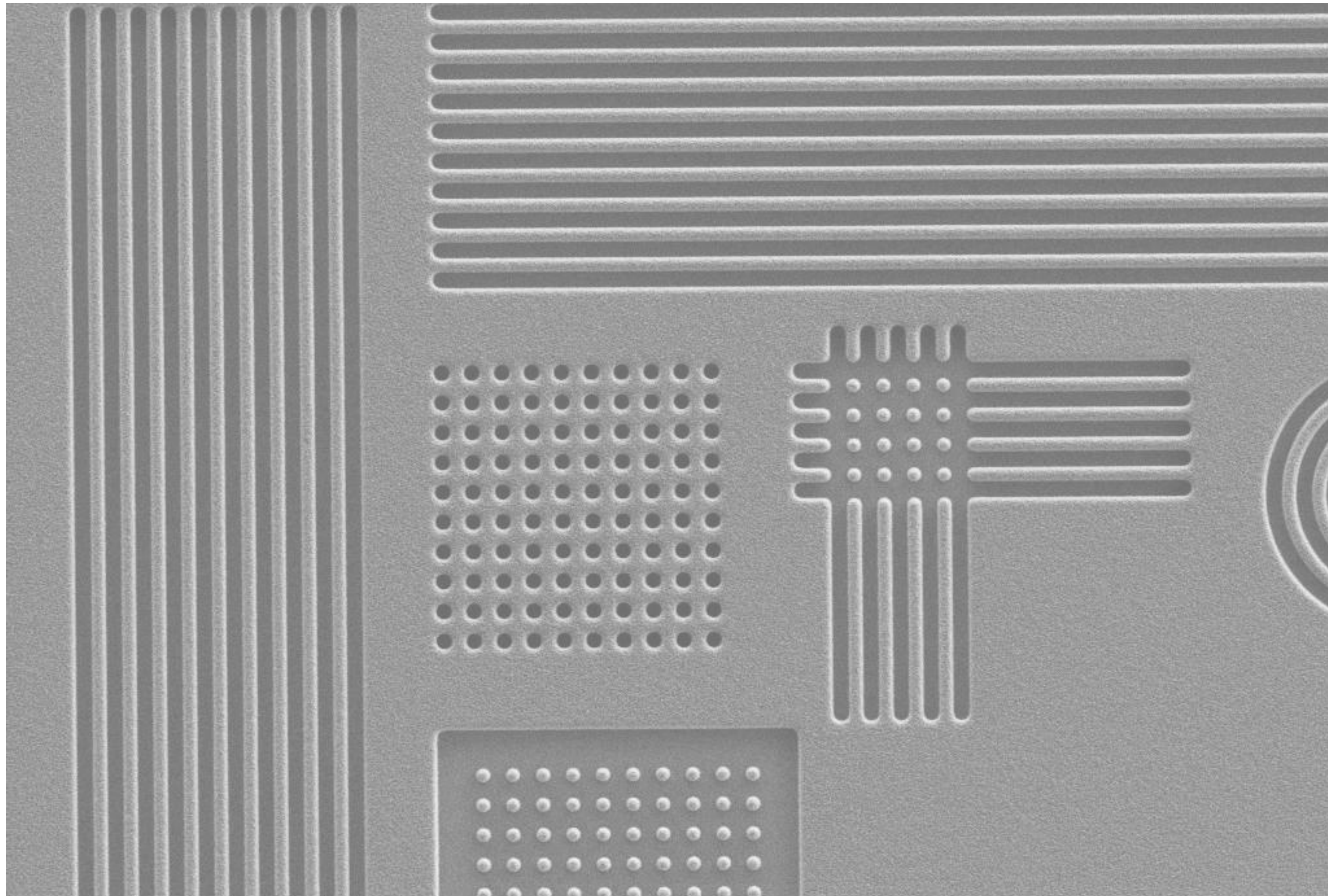
Lines and Spaces of the 390 nm thick JSR M230Y



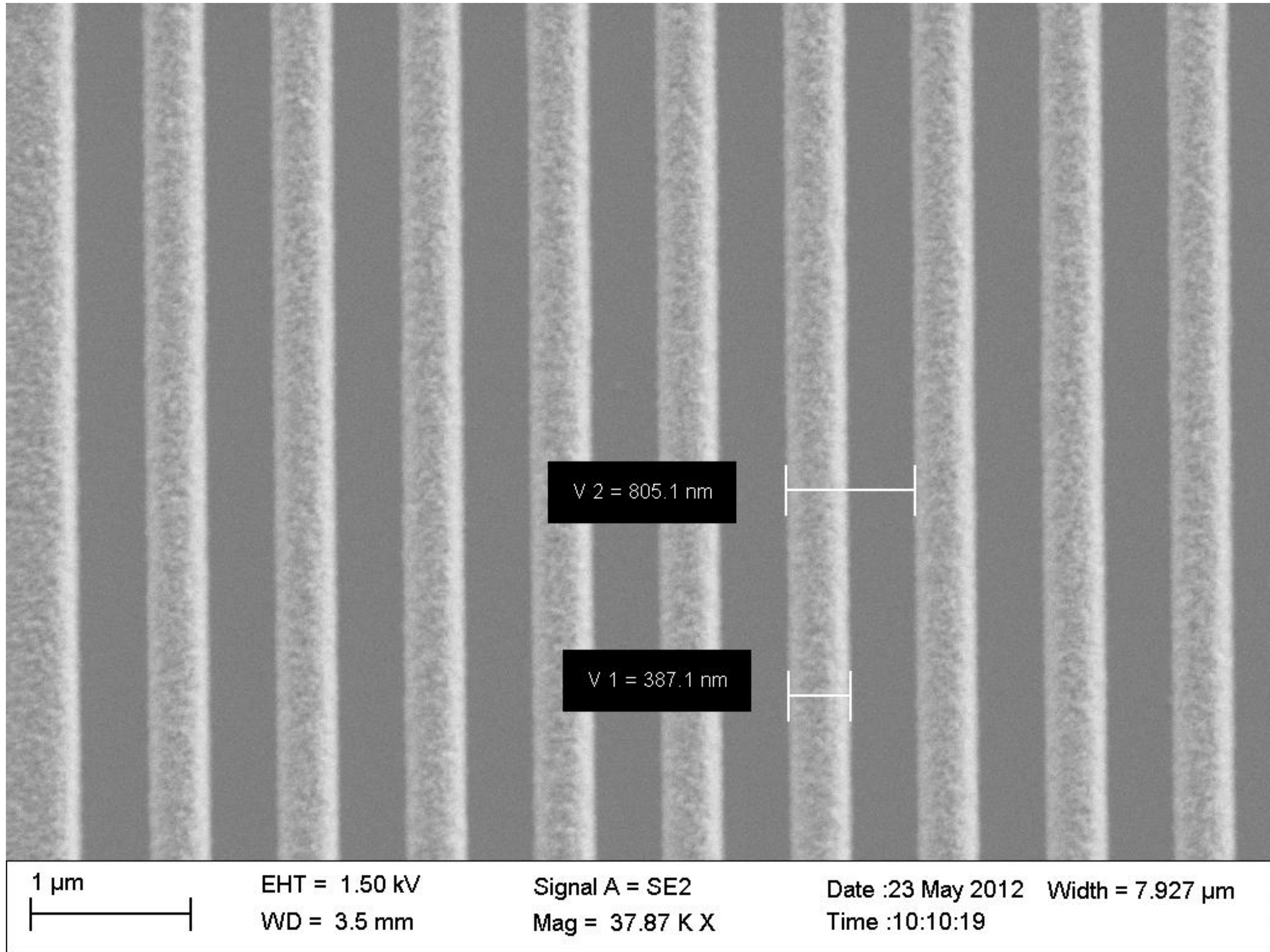
Summary Super Illumination

- Linewiths down to 160 nm, but only lines/spaces
- More interference patterns

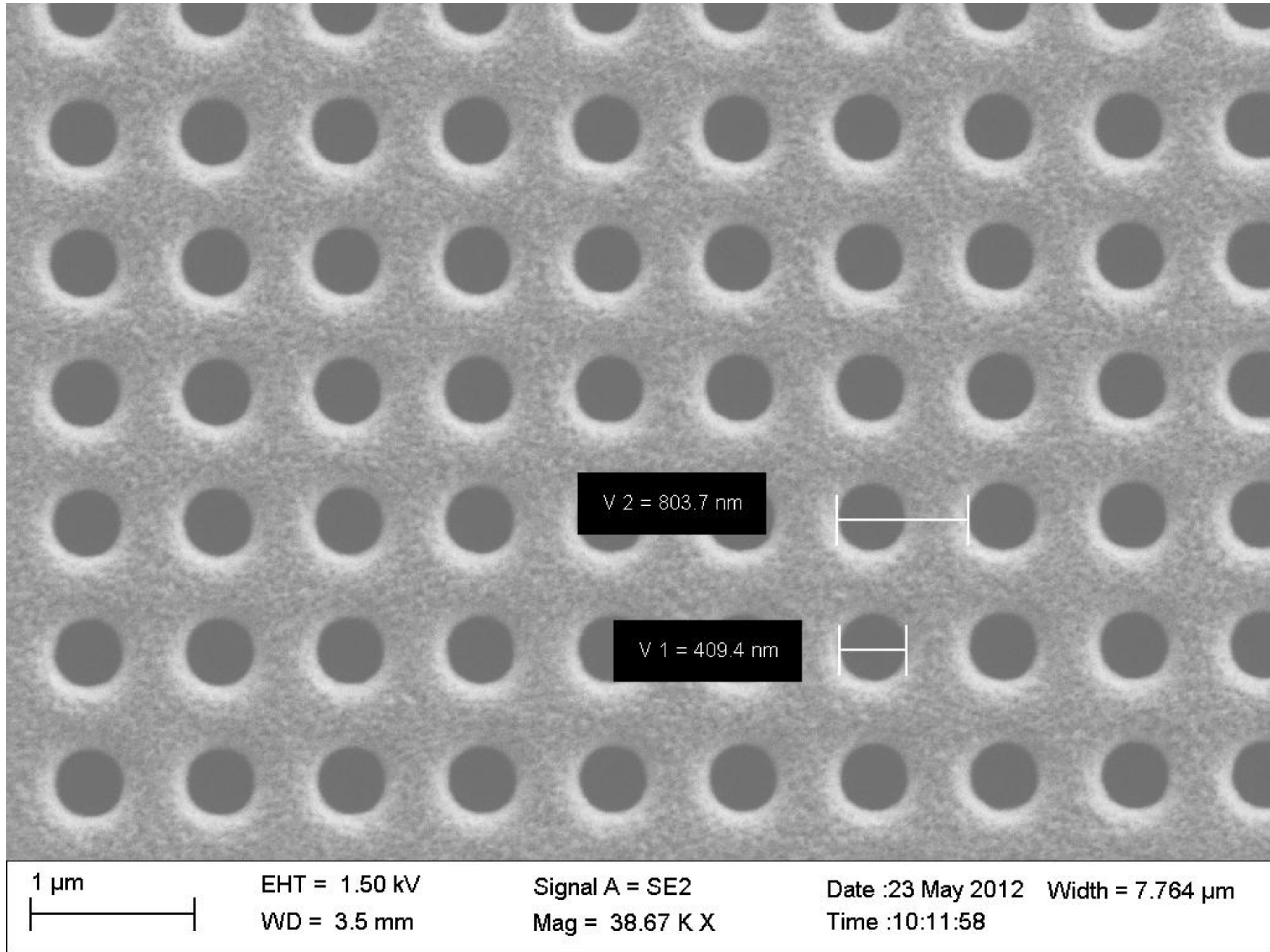
Negative process – 400 nm resist thickness



Negative 400 nm lines/spaces

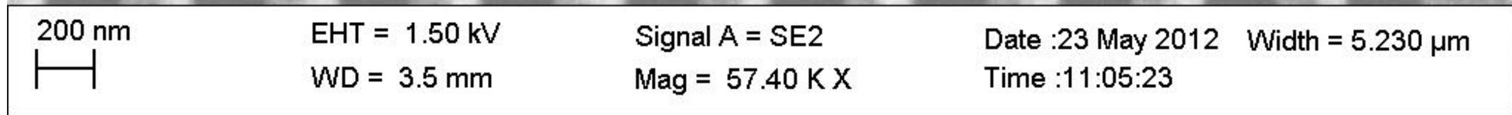


Negative 400 nm holes



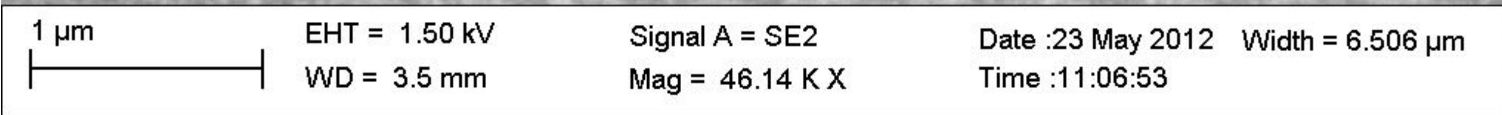
Negative 250 nm lines/spaces

V 2 = 495.4 nm
V 1 = 260.5 nm



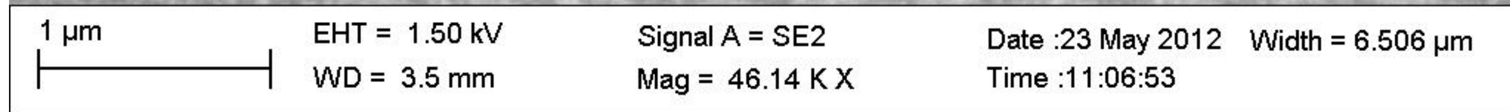
Negative 250 nm holes

V 1 = 133.4 nm



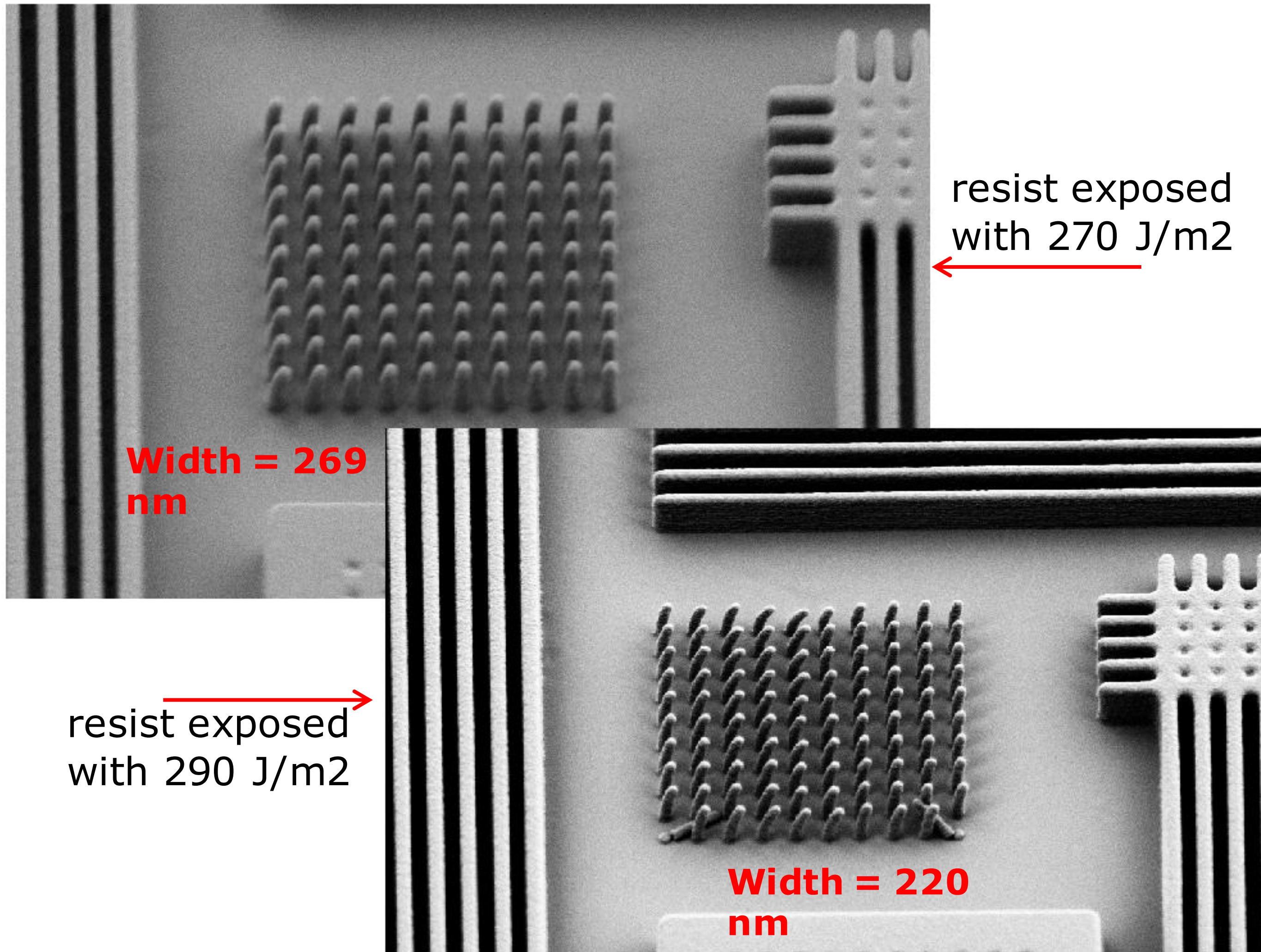
Negative 250 nm holes

V 1 = 133.4 nm



Resolution at 270 and 290 J/m^2

250 nm dots; 1 μm thick JSR-M35G;SEM 35⁰ tilted:



resist exposed with 270 J/m2

resist exposed with 290 J/m2

Metalized with 15 nm TiW

Highlight

- JBX9500 is the most accurate and highest scanning speed available point beam E beam writer

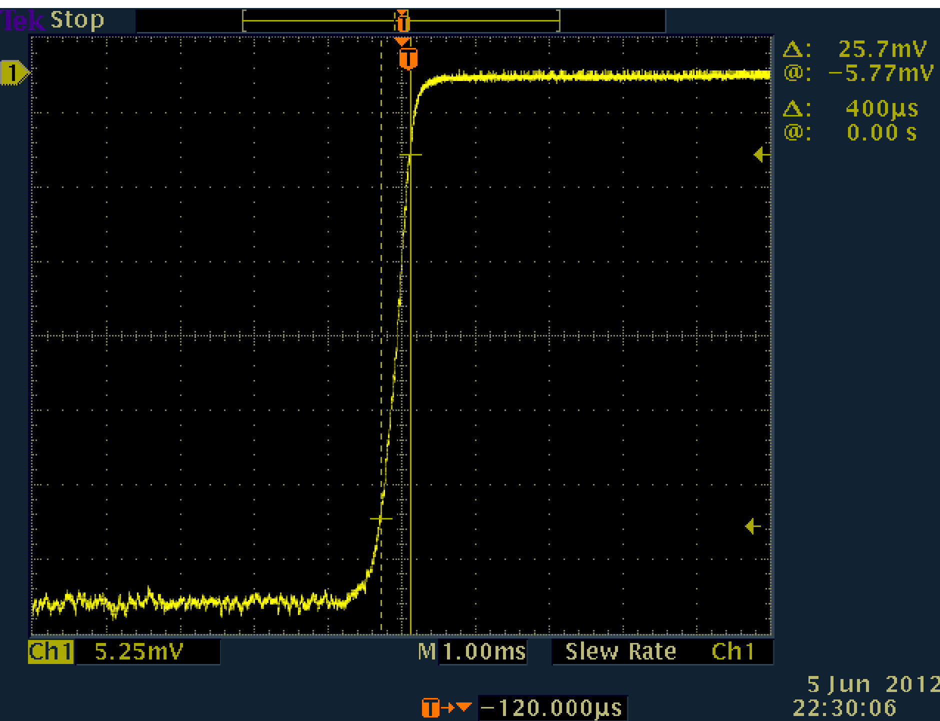
  - Stage accuracy within 6 inch area (133mmx133mm)
    - JBX9500 ≤ 11nm
    - Other E beam writers ≤ 20nm

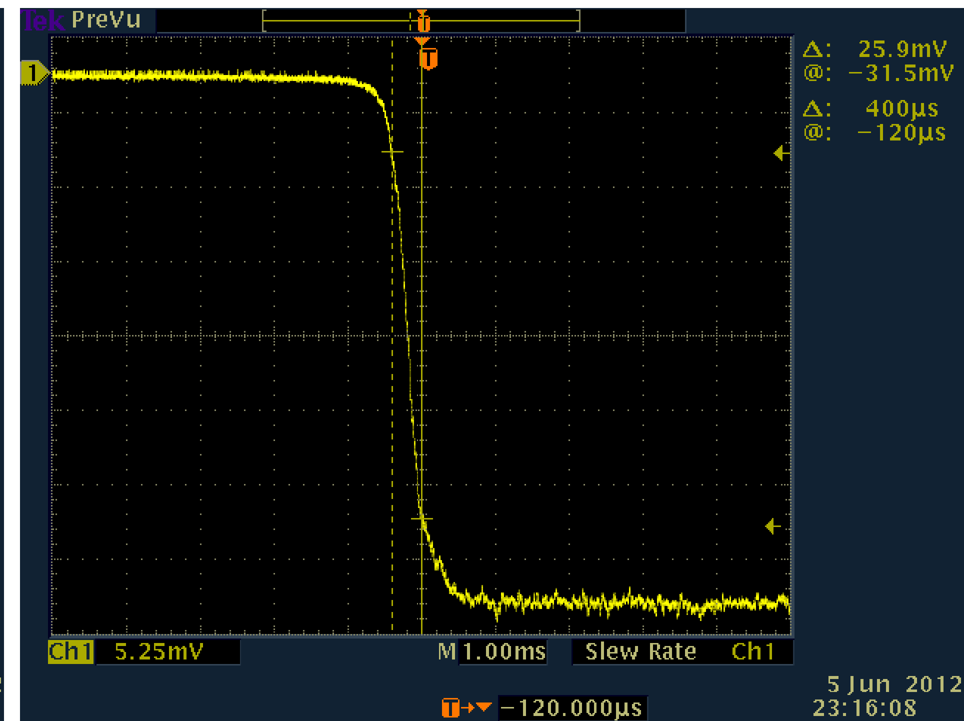
  - Scanning speed
    - JBX9500: 100MHz
    - Other E beam writers ≤ 50MHz

Specification of Jeol JBX9300 and New JBX9500

	JBX9300	JBX9500
Min. spot size	4nm	4nm
Min. line width	20nm	10nm
Max. scan speed	25MHz	100MHz
Max. writing field size	500um	1000um
Min. step size	1nm	0.5nm
Field stitch error	20nm	11nm
Position accuracy within 6inch area	20nm	11nm

JBX9500 Beam diameter measurement





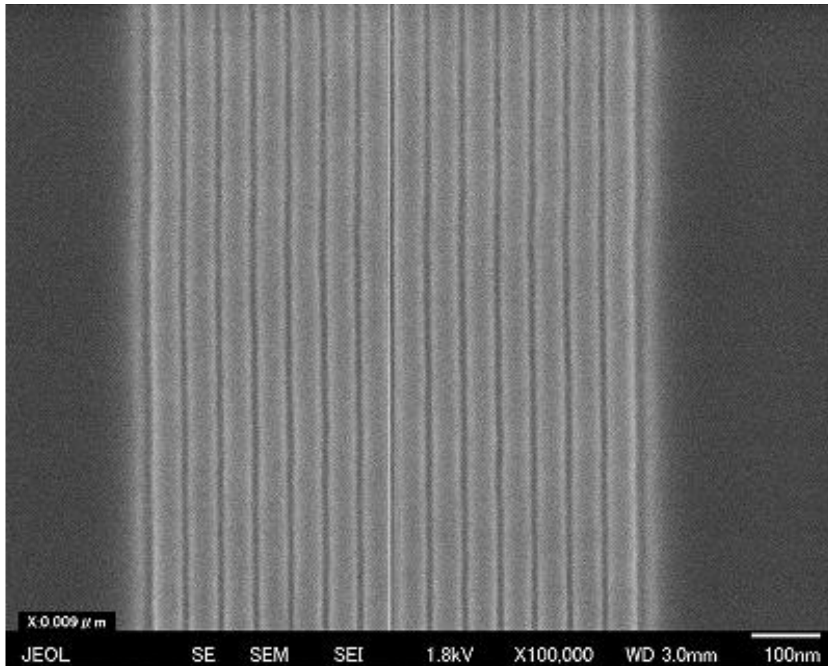
X diameter: 4nm

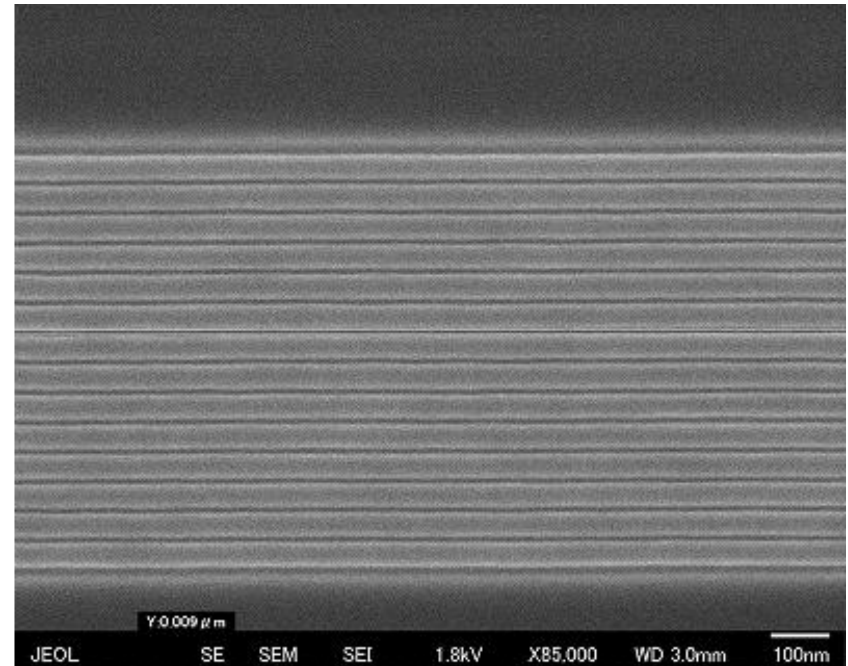
Y diameter: 4nm

---- Writing conditions ----

Current : 100pA

Min. Line width





---- Writing conditions ----

Field size:	1000um
Current:	200pA
Resist:	ZEP520A
Dose:	7580uC/cm^2
Shot pitch:	1nm

Spec= 10nm or less

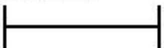
Results = Max: 9nm, in X and Y

18nm wide trench in the period of 44nm after 50nm deep dry etching on Si wafer

H 1 = 18.26 nm

H 2 = 44.08 nm

20 nm*



EHT = 5.00 kV
WD = 4.1 mm

Mag = 1396.67 K X
Width = 214.9 nm

Signal A = InLens

Date :7 Sep 2012

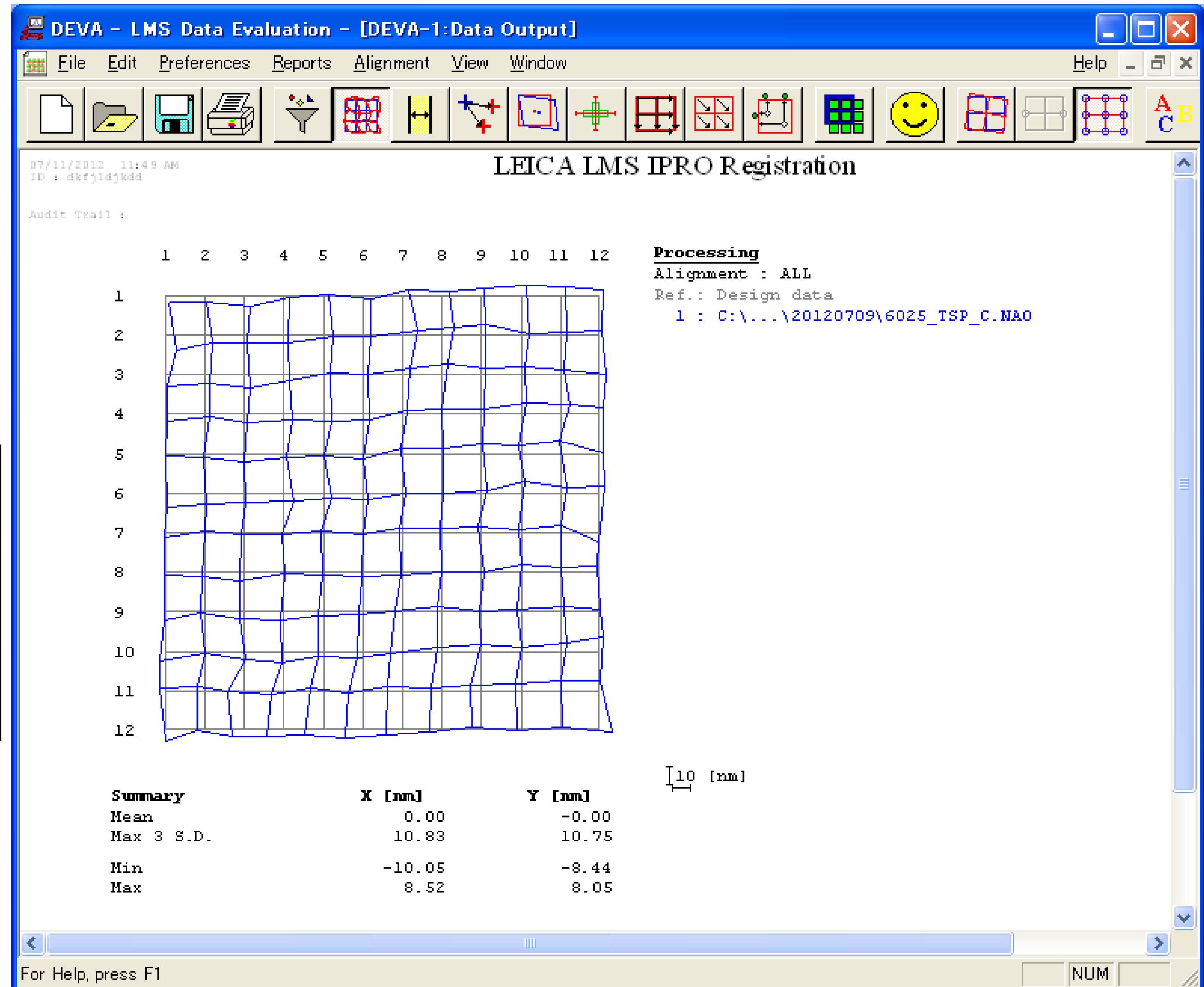
10nm position accuracy within 132mmx132mm on 6 inch Quartz mask plate

---- Writing conditions ----

Dose:	100uC/cm^2
Current:	2nA
Resist:	ZEP7000
Area:	132mm x 132mm

Spec= +/-11nm or less

Results	
Max.	Min.
8.52nm	*-10.05nm*



Thermal Oxide Quality Problem – too low break-down voltage

In general:

All processed wafers need to be RCA cleaned before entering any of the furnaces.

New rule:

New wafers need to be RCA cleaned before entering the following furnaces:

A1 Boron drive-in

A2 Boron pre-dep

A3 Phosphorous drive-in

A4 Phosphorous pre-dep

C1 Anneal-oxide (except PECVD1 wafers)

C2 Gate oxide

Remember also to RCA clean a test wafer.

To avoid mistakes **all users must get an extra training** before using the furnaces.

Please contact the Furnace Group (furnace@danchip.dtu.dk) for more information.

Ellipsometer

- Signed contract received yesterday
- Expected delivery: May 31st

Furnace with reducing atmosphere

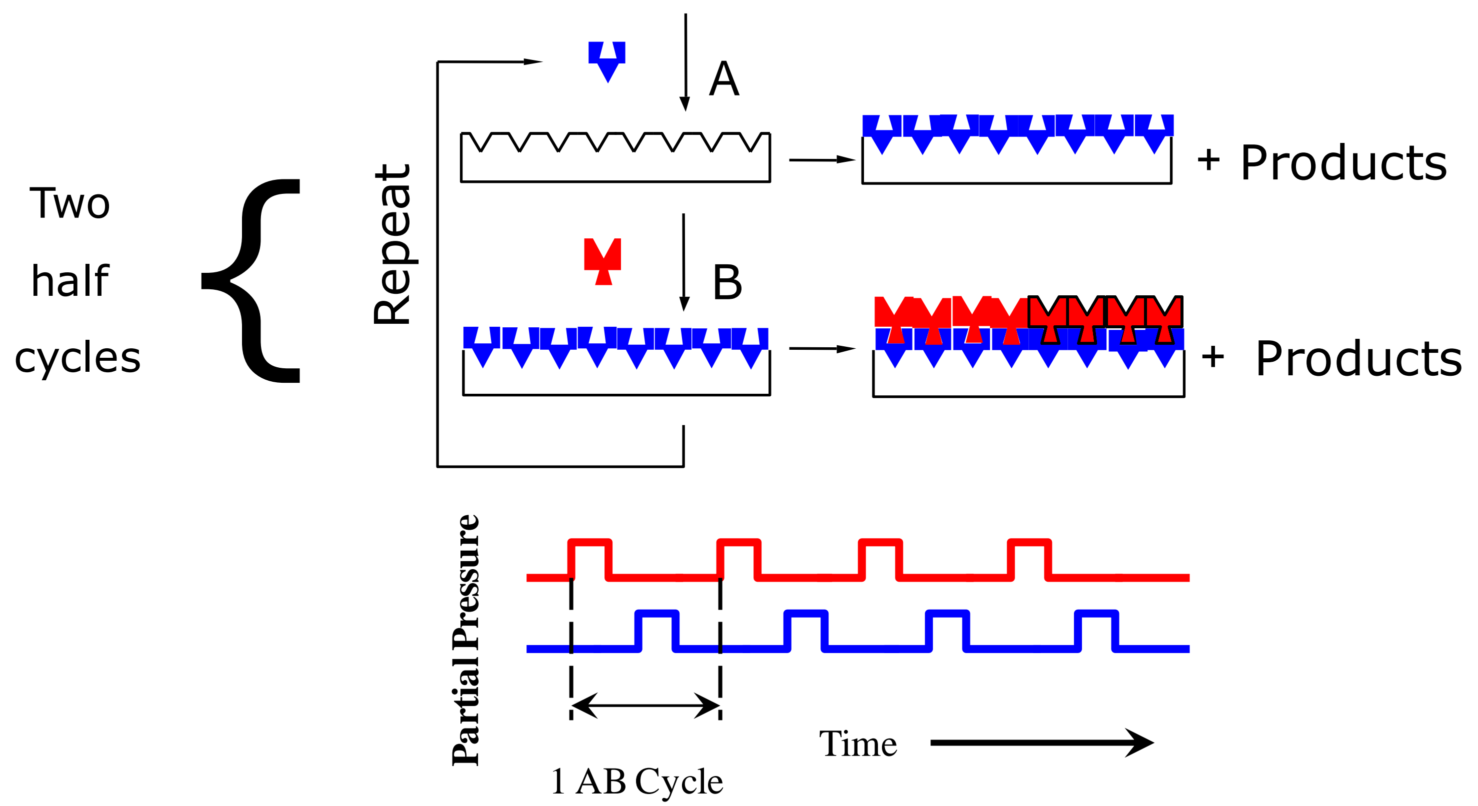
Candidate: PEO–604 (ATV)

- Multi-purpose process furnace with vacuum capability
- Capacity: 50 x 200 mm wafers
- Process temp: 1100 C, rate < 100 C/min
- Multi-purpose: Easy swap of quartz glass
- Ultimate vacuum: ~ 10^{-6} mbar
- Reducing atmosphere: **Max 4% H_2 / N_2**
- O_2 < 1ppm

Budget Quote: ca. 170 kEURO (incl. 2 gasses)

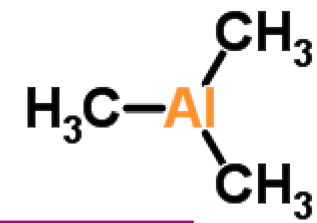
Atomic Layer Deposition:

Sequental, self-limiting surface reactions



ALD – Examples of precursors

TMA: Trimethylaluminum



- ALD Precursor Availability vs. periodic table

IA																	VIIIB
H	IIA											IIIB	IVB	VB	VIB	VIIB	He
Li	Be											B	C	N	O	F	Ne
Na	Mg	IIIA	IVA	VA	VIA	VIIA	[--------VIIIA-------]			IB	IIB	Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba		Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra		Rf	Db	Sg	Bh	Hs	Mt	Uun				Uuq				
			La	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
			Ac	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

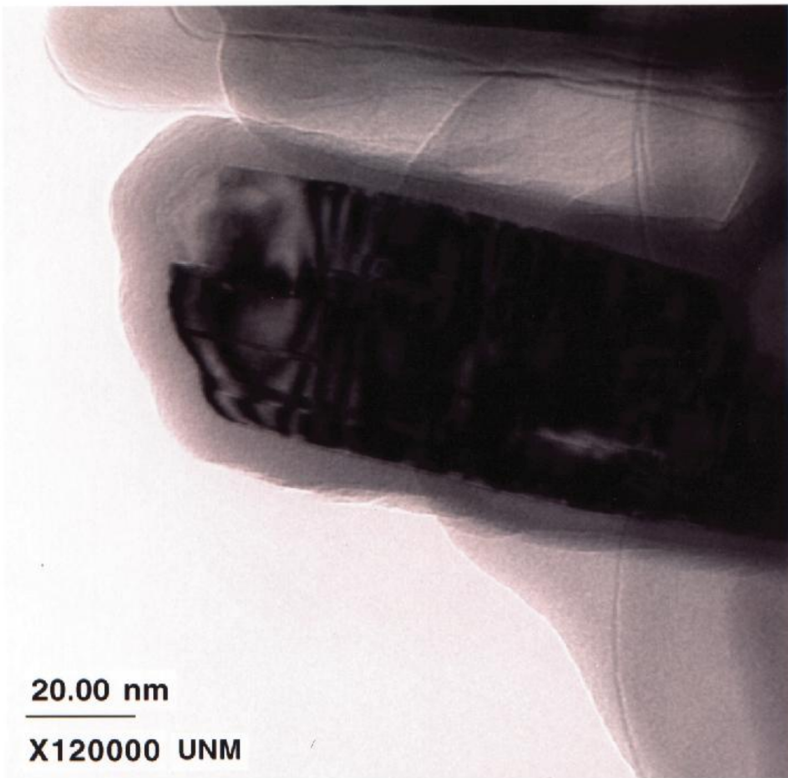
processes are used in volume manufacturing

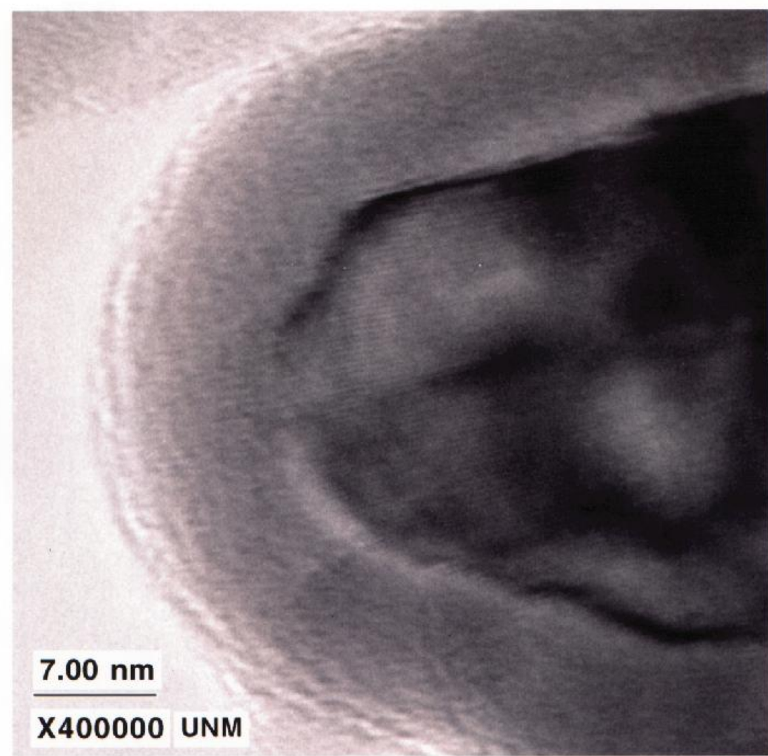
Processes in pilot phase (industrially)

Others

DTU

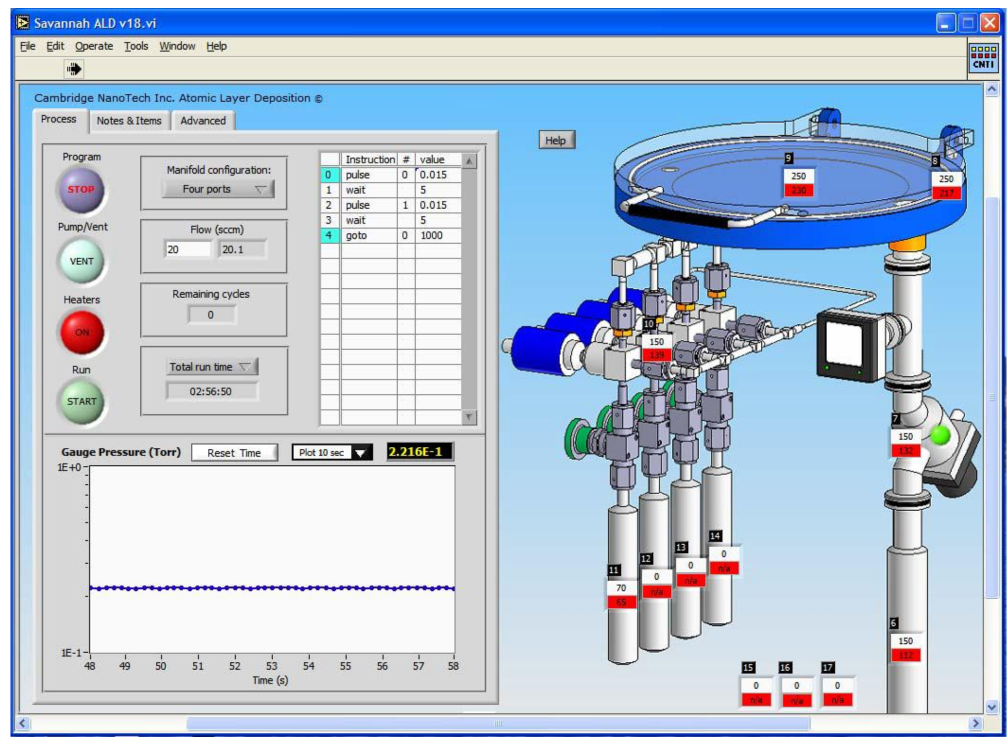
Example: Ultrathin conformal Al_2O_3 film on BN particles (Ferguson, Thin Solid Films, 371, 95 (2000))





Thermal ALD – Example of Tool

Cambridge Nanotech Inc: Savannah-100



Budget: ca. 1 MDKK

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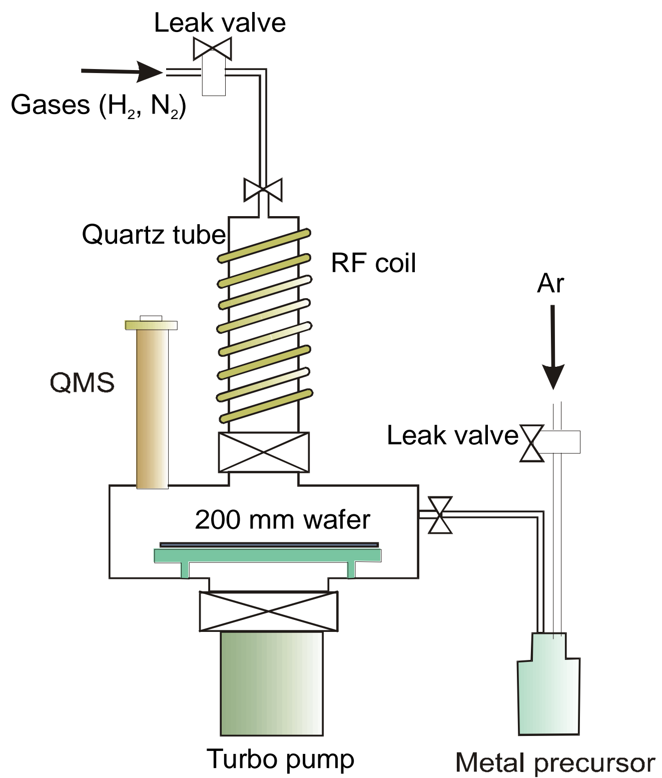
Plasma ALD – Example of Tool

Cambridge Nanotech Inc: Fiji F200



Budget: ca. 2.2 MDKK