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| Objective |
| Batch name: Process template |
| This process flow is a guideline on how to spin coat, expose, and develop AZ nLOF 2020 on 100 mm substrates such as Si, SiO2 and Borofloat, using automatic spin coater, mask aligner and automatic developer.  This is an example process flow to be used as a template. It should contain:   * The objective of the process * Substrates/samples used in the flow - both actual samples to be processed (device wafers) and any monitor samples for the different process steps * The Process flow main processes and steps * Recommended: Figures illustrating the sample before and after each main process step   How to use this template (works only with the .dotx template file):   * Fill out the fields in the header * Add process steps by using Quick Parts under Insert (your cursor should be located at the beginning of the next (empty) step) Select the “Process Step” item * Other document parts can be inserted the same way: Substrates, Figures, etc. * The Content (TOC) on the last page is an option, but provides a nice overview for very long process flows |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Substrates | | | | | | | | | | |
| Substrate | Orient. | Size | | Doping/type | Polish | thickness | Box | Purpose | # | Sample ID |
| Silicon | <100> | | 100 mm | n (Phos.) | SSP | 525 ±25 µm |  | Device wafers | 2 | S1-S2 |
| Silicon | <100> | | 100 mm | n (Phos.) | SSP | 525 ±25 µm |  | Test wafers | 1 | T1 |

Comments: Number of wafers is for illustration only

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| --- | --- | --- | --- |
| Figures | | | |
| Figure | Caption | Step | Figure |
|  | After SiO2 dep  Not part of this process flow example | 2.1 |  |
|  | After lithography | 3.5 |  |
|  | After BHF etch  Not part of this process flow example | 4.1 |  |
|  | After resist strip  Not part of this process flow example | 4.4 |  |
|  | After lithography  Not part of this process flow example | 5.6 |  |
|  | After metal deposition  Not part of this process flow example | 6.1 |  |
|  | After lift-off  Not part of this process flow example | 6.2 |  |

Comments:Click here to enter text.

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| --- | --- | --- | --- |
| Step Heading | Equipment | Procedure | Comments |
| 1. Preparation | | | **All wafers** |
| * 1. Wafer selection | Wafer box | Take the wafers from the storage and put them in a wafer box. | Note the wafer IDs in the batch traveler |
| 1. SiO2 deposition | | | **All wafers** |
| * 1. Not part of this process flow example |  |  |  |
| 1. Lithography – standard | | | **All wafers** |
| * 1. Surface treatment | BHF dip  *Or*  Oven:  HMDS – 2 | BHF dip for Si substrates (BHF: 30 sec, H2O: 5 min)  HMDS treatment for Si, SiO2, and Borofloat  **Recipe:**  01 | For Si, choose BHF or HMDS  HMDS priming can also be performed inline on Gamma spin coaters |
| * 1. Coat wafers | Spin Coater: Gamma UV | **Resist:**  AZ nLOF 2020  **Spin:**  30 s @ 3300 rpm (for 2.0 µm)  **Softbake:**  60 s @ 110 °C  **Sequence gamma UV:**  2420 DCH 100mm nLOF 2um | **Inline HMDS priming:**  Gamma UV: 2421  Resist thickness can be measured on FilmTek or ellipsometer |
| * 1. Exposure | Aligner:  MA6 – 2 | **Mask:**  your mask  **Exposure mode:**  Soft contact  **Exposure dose:**  112 mJ/cm2  **Exposure time:**  10.2 s @ 11 mW/cm2 | Further information is available on labadviser:  https://labadviser.nanolab.dtu.dk/index.php?title=Specific\_Process\_Knowledge/Lithography |
| * 1. Post exposure bake | Developer: TMAH UV-lithography | **Post Exposure Bake:**  60 s @ 110 °C  **Sequence:**  PEB only: 2001 DCH PEB 110C 60s  PEB + DEV: 3001 DCH 100mm PEB60s@110C+SP60s  PEB + DEV: 3005 DCH 100mm PEB60s@110C+SP30s | 120 s PEB is better for Borofloat. May require lower exposure dose.  PEB and development is typically done simultaneously |
| * 1. Develop | Developer: TMAH UV-lithography | **Development in TMAH (AZ 726 MIF):**  single puddle, 30 s or 60 s  **Sequence:**  DEV only: 1001 DCH 100mm SP 30s  DEV only: 1002 DCH 100mm SP 60s  PEB + DEV: 3001 DCH 100mm PEB60s@110C+SP60s  PEB + DEV: 3005 DCH 100mm PEB60s@110C+SP30s | Choose 60 s development for extra undercut (lift-off).  PEB and development is typically done simultaneously |
| * 1. Inspection | Optical microscope | Check pattern and alignment marks |  |
| 1. SiO2 etch | | | **All wafers** |
| * 1. Not part of this process flow example |  |  |  |
| 1. Lithography – Lift off | | | **All wafers** |
| * 1. Not part of this process flow example |  |  |  |
| 1. Aluminum pattern | | | **Only device wafers!!** |
| * 1. Not part of this process flow example |  |  |  |
| 1. Linewidth measurement | | | **All wafers** |
| * 1. Not part of this process flow example |  |  |  |

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